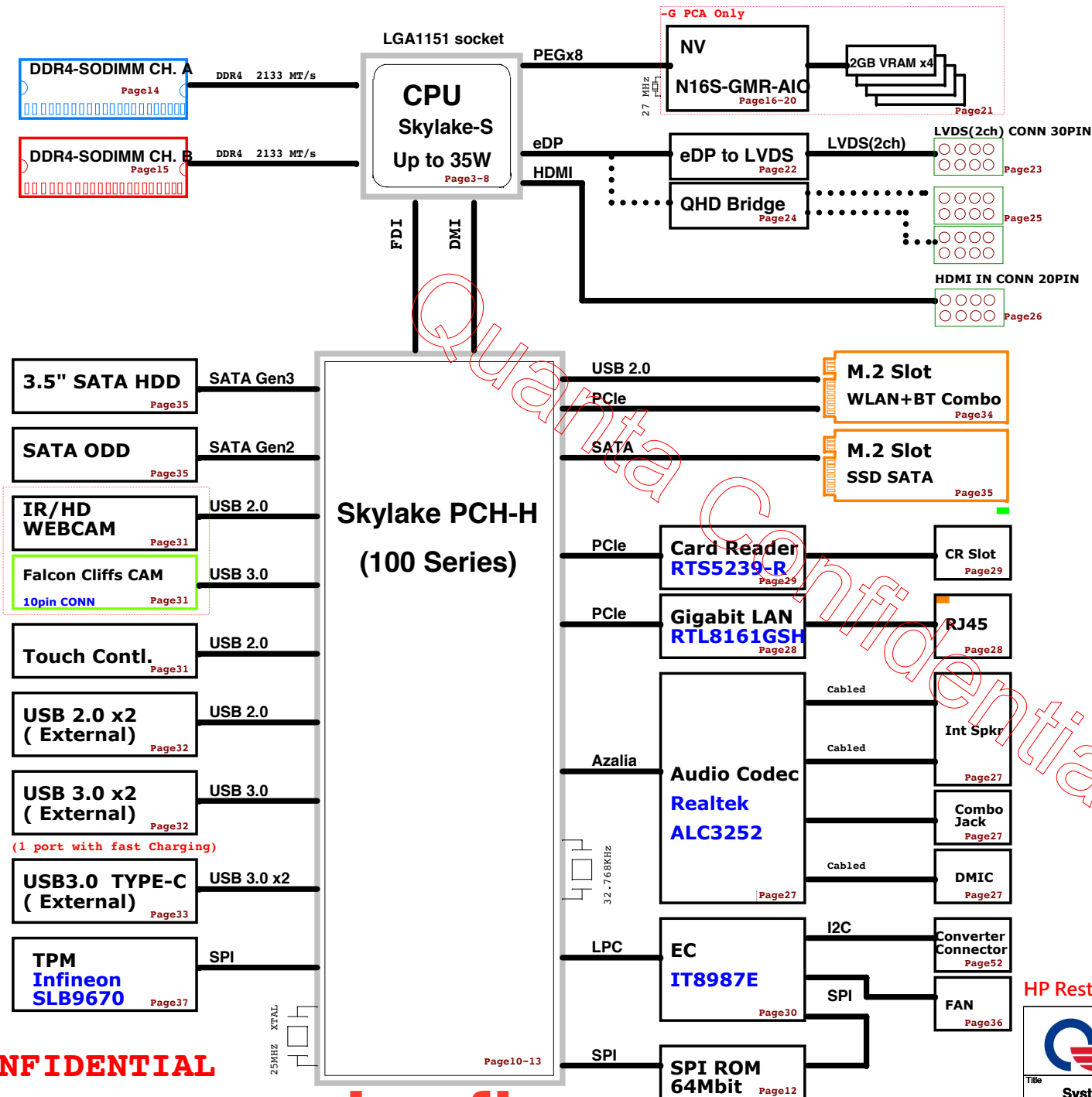


# HP Saipan System Block Diagram

01



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Quanta Computer Inc.

Project: HP-Saipan

Title: System Block Diagram

Size: Document Number: Rev A

Page Modified: Thursday, December 17, 2015 Sheet 1 of 61

## Voltage Rails

02

Power Rail	Voltage	S0	S3	S4	S5	PCU	G3	Ctl Signal
+RTC_VCC	3V	ON	ON	ON	ON	ON	ON	
+VIN	19V	ON	ON	ON	ON	ON	ON	Adapter in
+5V_ALW	5V	ON	ON	ON	ON	ON	ON	Int. LDO
+3V_ALW	3.3V	ON	ON	ON	ON	ON	ON	Int. LDO
+3V_AUX	3.3V	ON	ON	ON	ON	ON	OFF	LDO
+5V_S5	5V	ON	ON	ON	ON	OFF	OFF	S5_ON
+3V_S5	3.3V	ON	ON	ON	ON	OFF	OFF	S5_ON
+1.8V_S5	1.8V	ON	ON	ON	ON	OFF	OFF	S5_ON
+1V_S5	1.0V	ON	ON	ON	ON	OFF	OFF	PG_+1.8V_S5
+VCCST_VCCPLL	1.0V	ON	ON	OFF	OFF	OFF	OFF	S3_ON
+VDDQ	1.35V	ON	ON	OFF	OFF	OFF	OFF	S3_ON
SMDDR_VTERM	0.75V	ON	ON	OFF	OFF	OFF	OFF	DDR_VTT_CNTL
+5V	5V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1
+3V	3V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1
+12V	12V	ON	OFF	OFF	OFF	OFF	OFF	MAIN_ON1
+VCCIO	0.95V	ON	OFF	OFF	OFF	OFF	OFF	PG_MAIN
+VCCSA	1.05V	ON	OFF	OFF	OFF	OFF	OFF	PG_+VCCIO
+VCCGT	0.65~1.3V	ON	OFF	OFF	OFF	OFF	OFF	VR_ON
+3.3V_VGA	3.3V	ON	OFF	OFF	OFF	OFF	OFF	EN_+3.3V_VGA
+1.05V_VGA	1.05V	ON	OFF	OFF	OFF	OFF	OFF	PG_+3.3V_MAIN
+VGA_CORE	0.8~1.15V	ON	OFF	OFF	OFF	OFF	OFF	PG_+3.3V_MAIN
+1.35V_VGA	1.35V	ON	OFF	OFF	OFF	OFF	OFF	EN_+1.35V_VGA
+VCCCORE	0.65~1.3V	ON	OFF	OFF	OFF	OFF	OFF	VR_ON

RTC Batt, PCH , EC

LED

EC

System

PCH, USB, 3D WebCAM, Touch Panel, USB Charger

PCH, XDP, SPI flash ROM,NGFF LAN

PCH, XDP, NGFF LAN

PCH

CPU, PCH, XDP

DDR4, CPU DDR4 I/O

DDR4

HDD, ODD,Audio AMP,Panel VCC,FAN

PCH, Audio, Card Reader, TPM, FHD CAM

3.5" HDD

CPU

CPU

CPU

dGPU

dCPU

dGPU

dGPU, VRAM

CPU

## Schematic "Value" Definition

Intel Platform Saipan-G and Saipan-U			DB/SI/PV Stage		MP		ALL STAGE	
By Value format	Description	Auto BOM Control	UMA	Discrete N16S GPU	UMA	Discrete N16S GPU	QHD PANEL	FHD PANEL
XX	Install	V	V	V	V	V		
*XX	Non-Install	V						
PROTO@XX	Install in Pre-production only	V	V	V				
MP@XX	Install in MP only	V			V	V		
DIS@xx	Install Discrete (DGPU) only	V		V		V		
UMA@xx	Install UMA	V	V		V			
QHD@xx	QHD panel	V	V	V	V	V	V	
FHD@xx	FHD panel	V	V	V	V	V		V

\*\*\*Board ID and VRAM ID by manual control

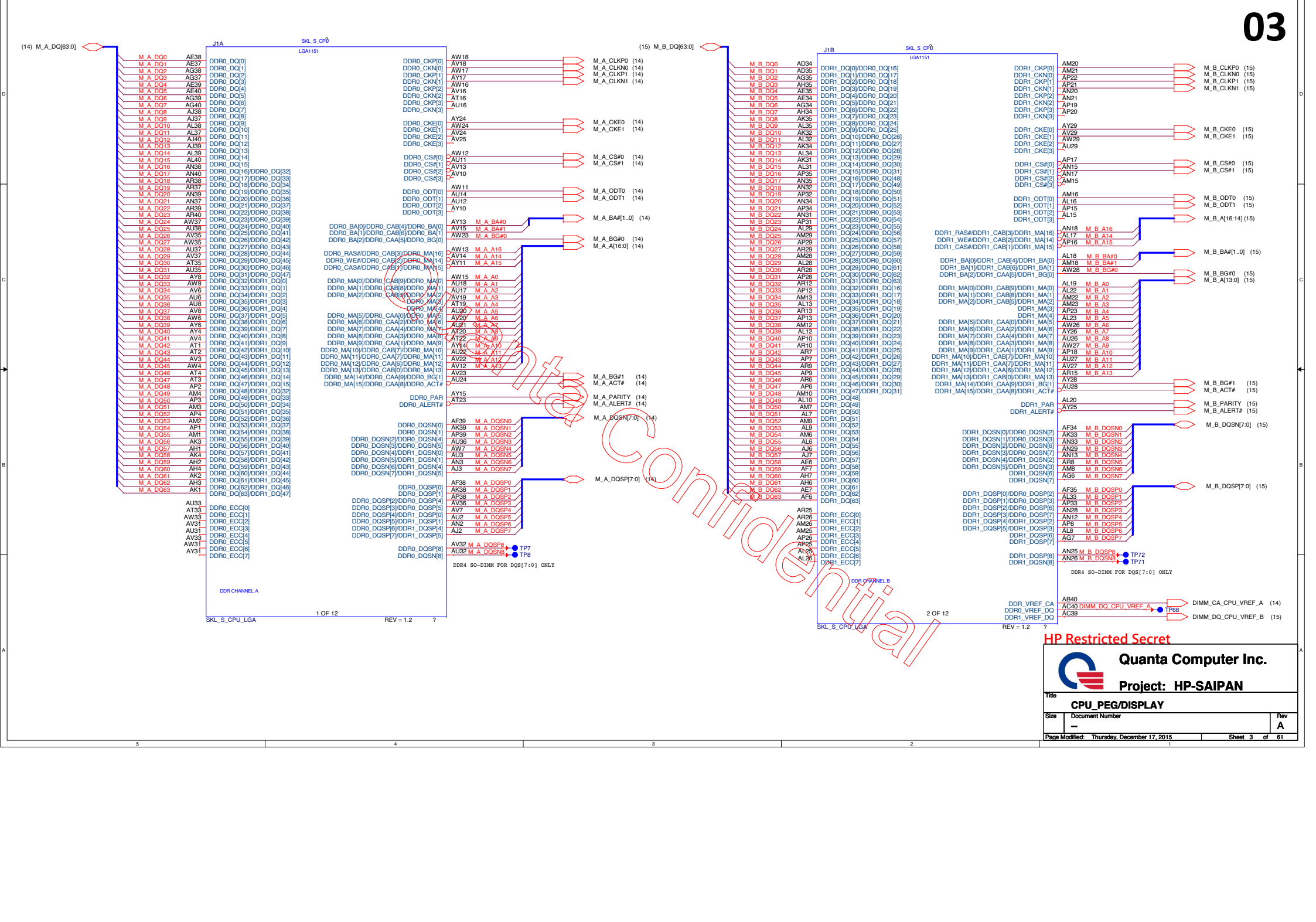
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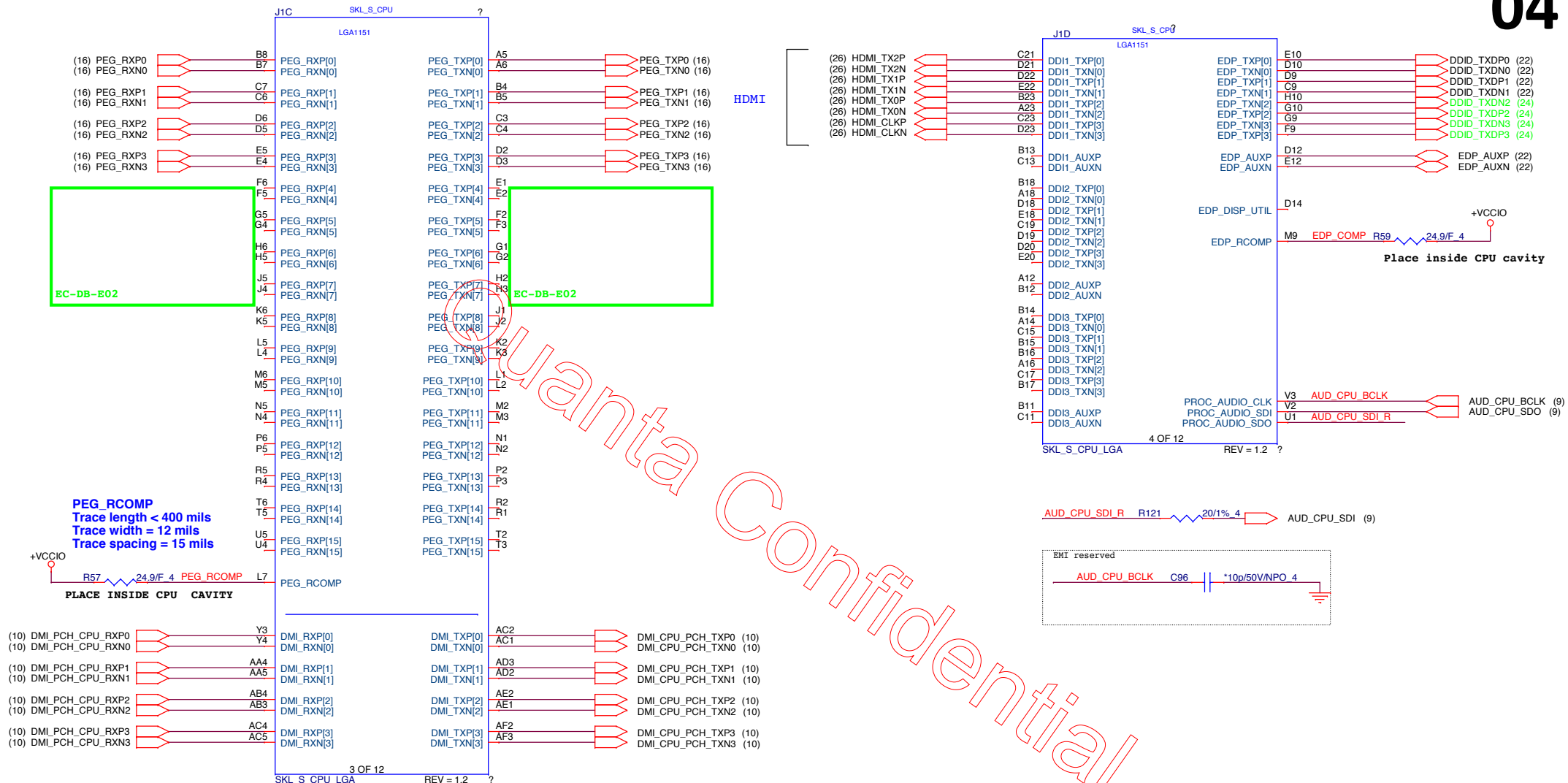


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Project: HP-Saipan

Title			Project: HP-SAFAN	
Power States & Value Definition				
Size	Document Number			Rev
				A
Page Modified: Thursday, December 17, 2015			Sheet 2 of 61	





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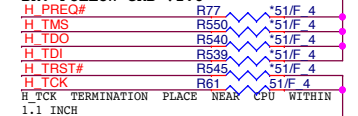
Project: HP-SAIPAN

Title		
CPU_PEG/DISPLAY		
Size	Document Number	Rev
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Page Modified: Thursday, December 17, 2015		
Sheet 4 of 61		

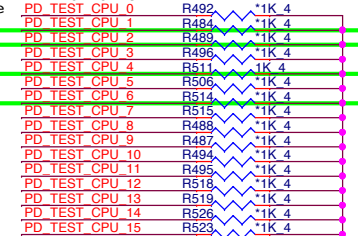


+VCCST\_VCCPLL

BK: FOLLOW CRB v1.0



BK: FOLLOW CRB 1.1



Unstuff R461 &amp; R462 for SPT-H

+3V\_S5

SKL\_CNL R6 \*10k/5% 4



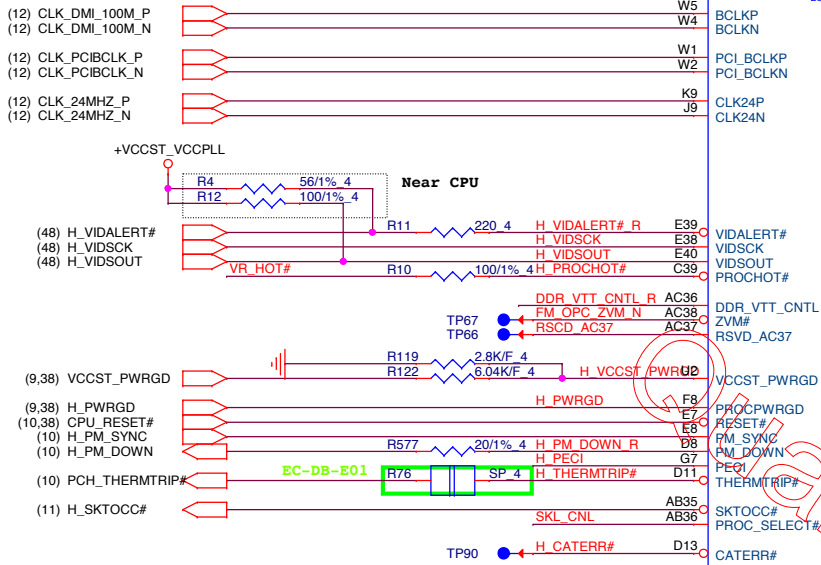
BK: CRB --&gt; NO THESE, NEED CONFIRM

+VCCST\_VCCPLL

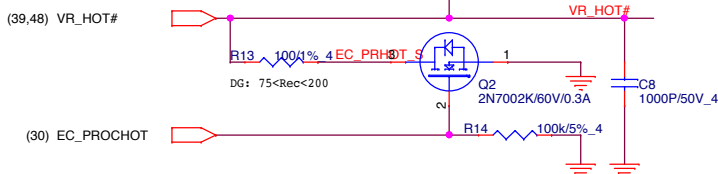
PCH\_THERMTRIP# R75 1k/5% 4

CRB: Close to SPT-H

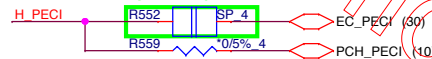
H\_PWRGD R564 \*10k/5% 4



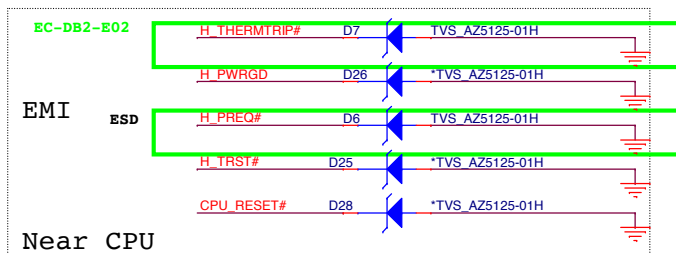
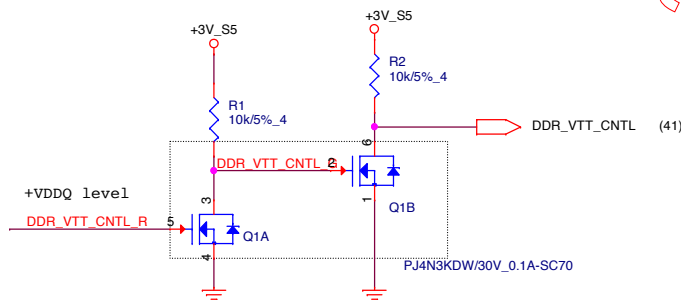
H\_PROHOT#



H\_PECI



DDR\_VTT\_CNTL



Near CPU

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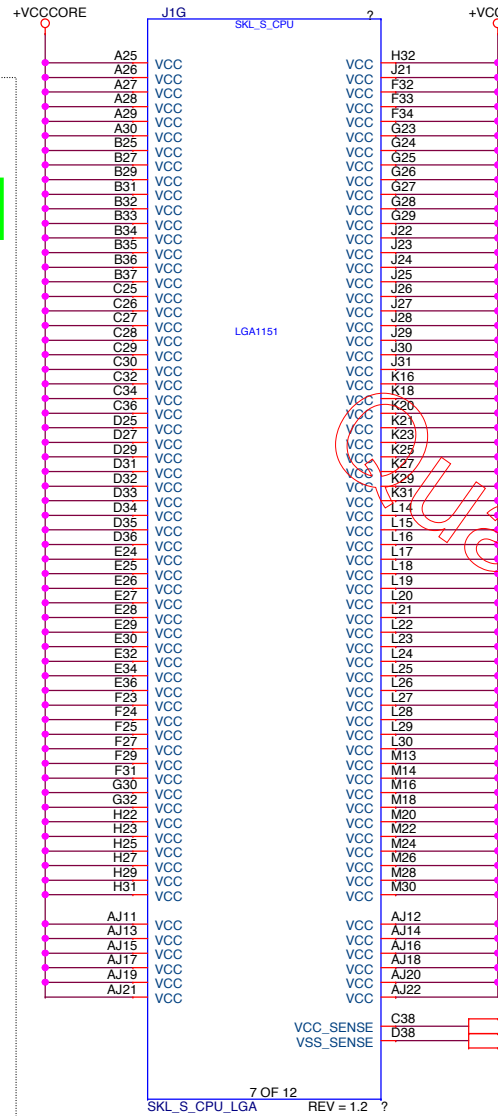
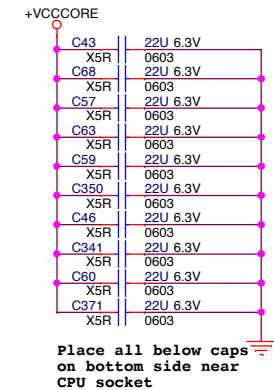
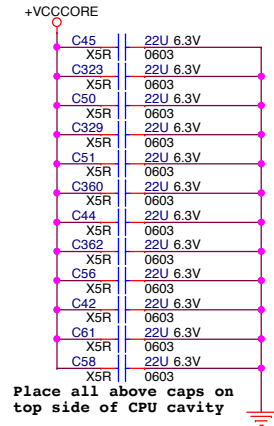
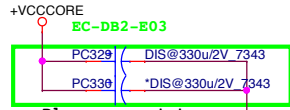
Title CPU MISC		
Size	Document Number	Rev A
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Page Modified: Thursday, December 17, 2015		Sheet 5 of 61

+VCCCPRE:  
Icc ( max ) : 66A  
Icc ( PS2 ) : 35A

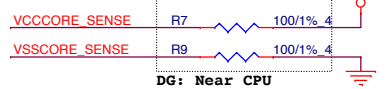
(7,47,48,49) +VCCCORE  
(47,48,50) +VCCGT



### Decoupling Capacitors

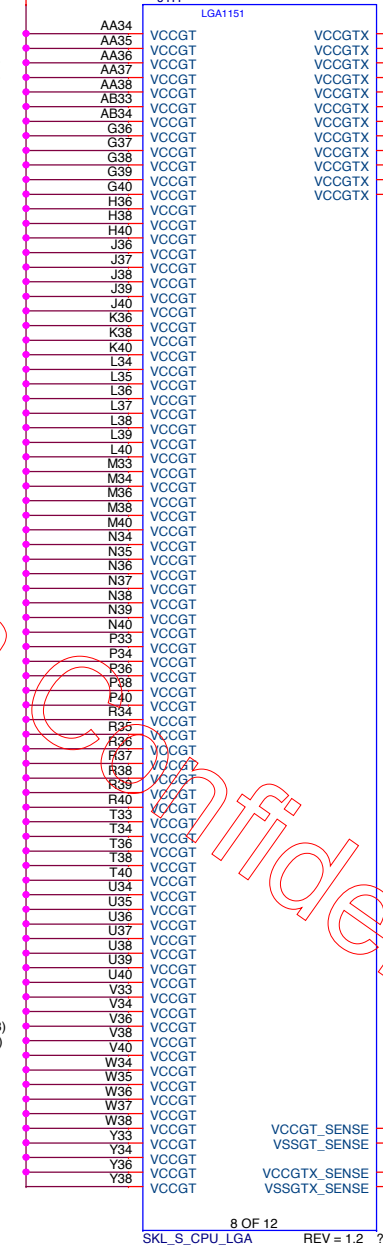


VCCCORE\_SENSE R8 0.5% 4 VSSCORE\_SENSE

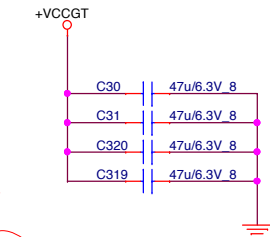
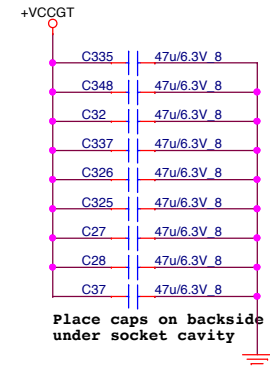
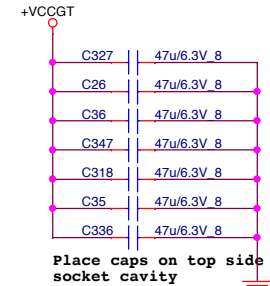


+VCCCPRE:  
Icc ( max ) : 40A  
Icc ( PS2 ) : 32A

+VCCGT



### Decoupling Capacitors



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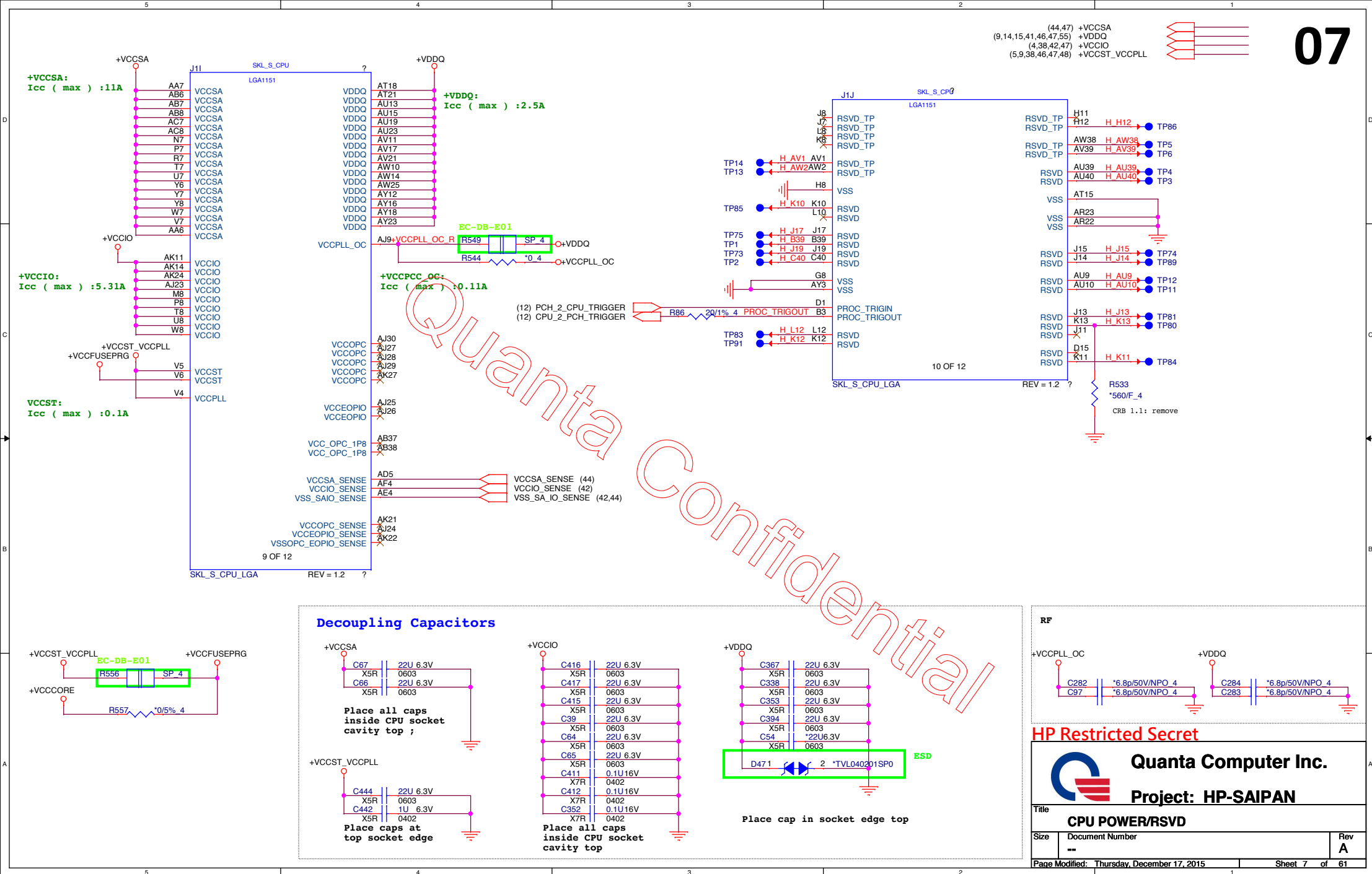


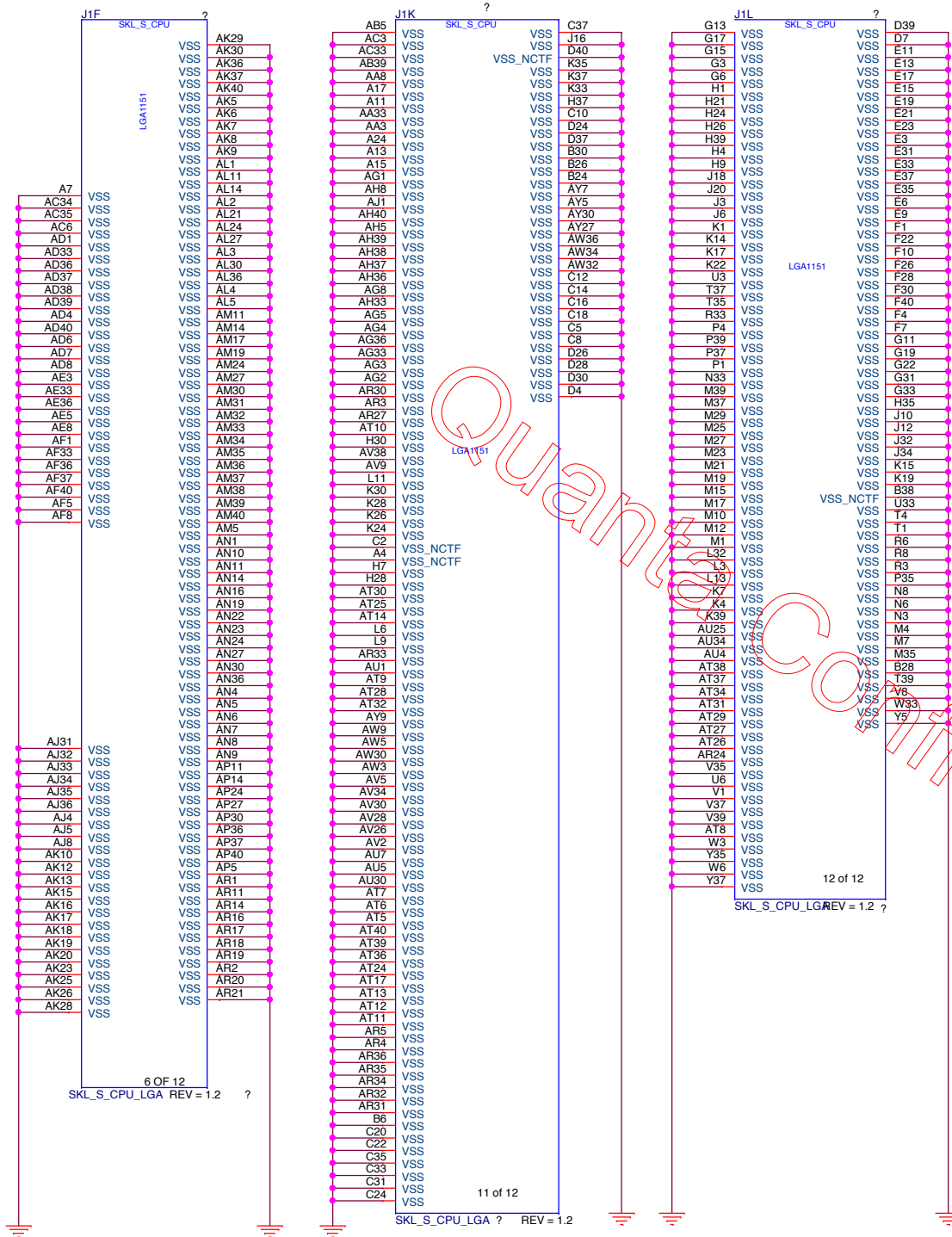
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Project: HP-SAIPAN

Title		
CPU POWER		
Size	Document Number	Rev
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Page Modified: Thursday, December 17, 2015		Sheet 6 of 61







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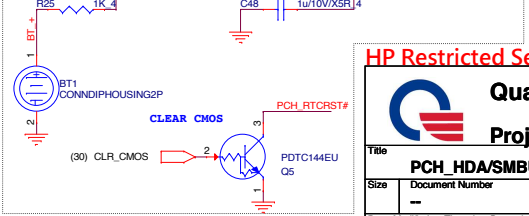
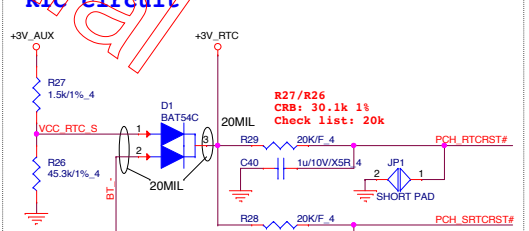
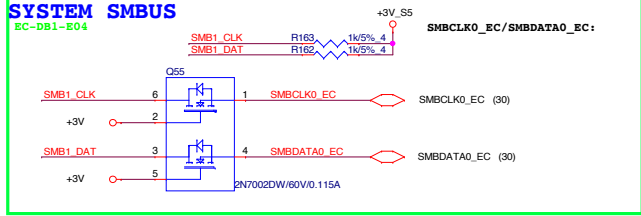
Project: HP-Saipan

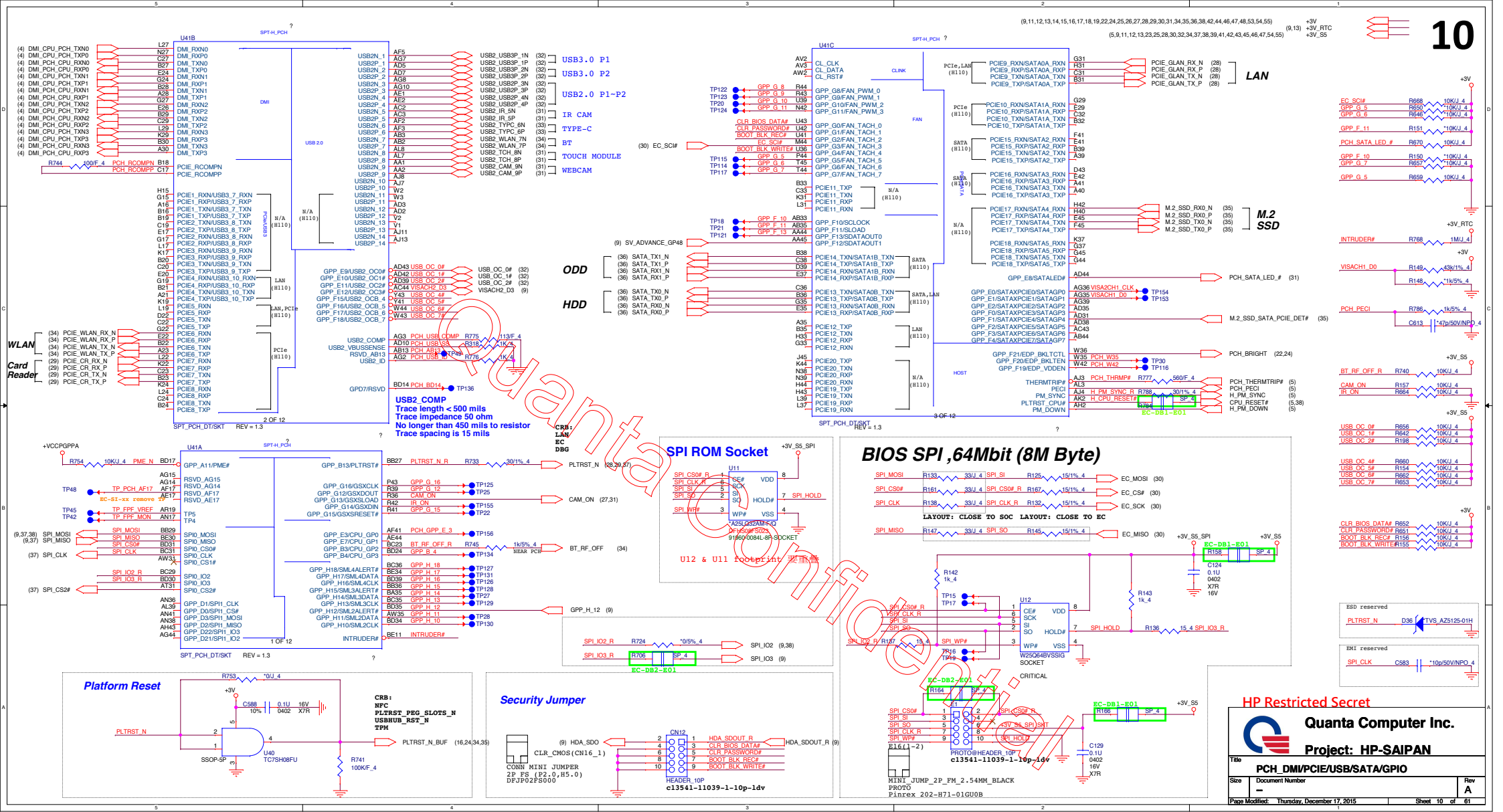
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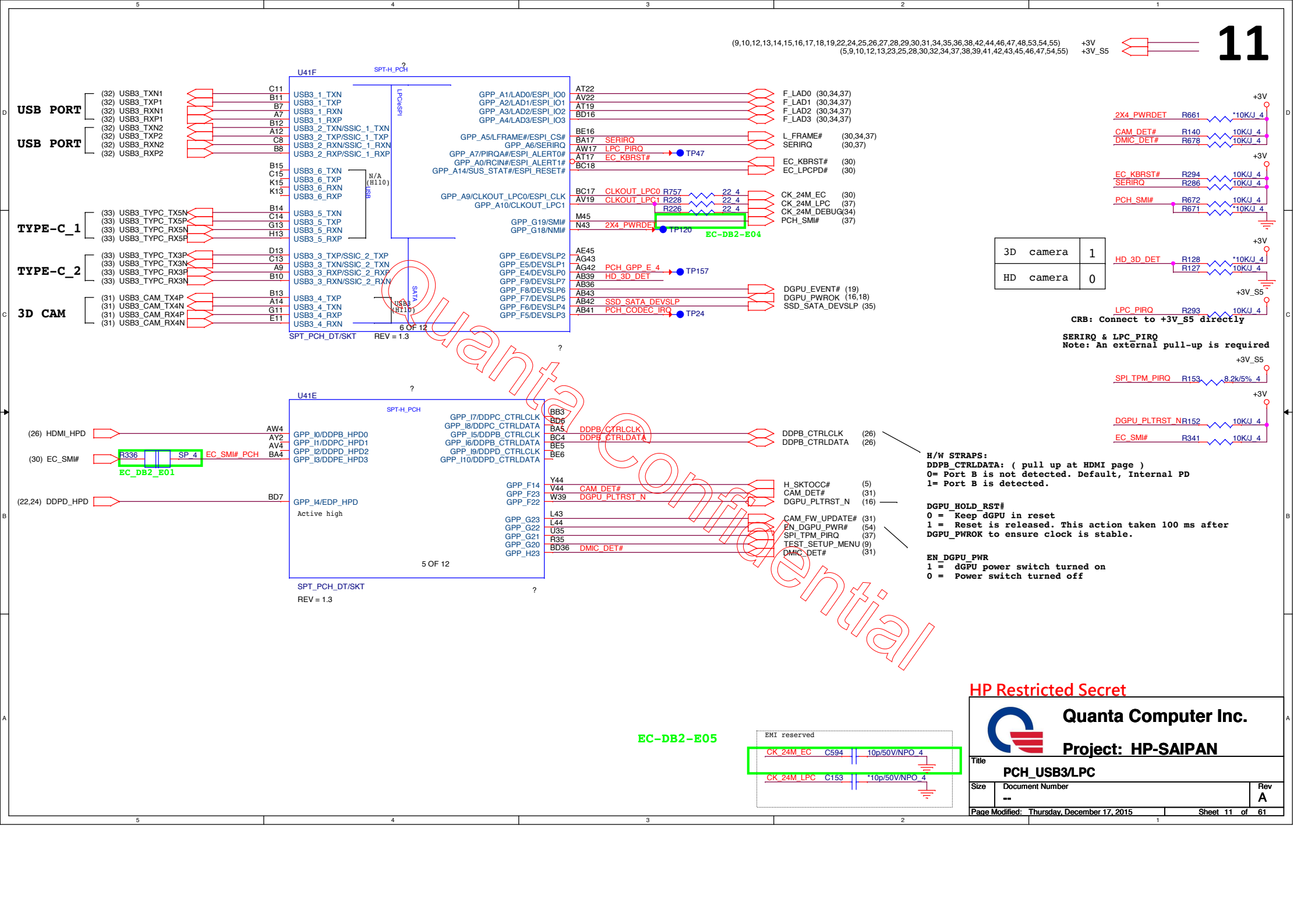


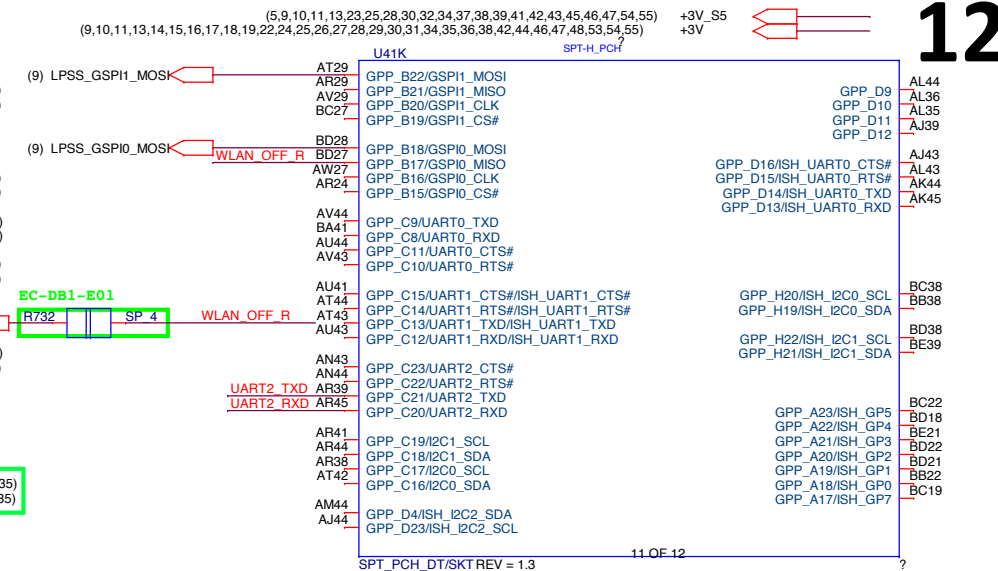


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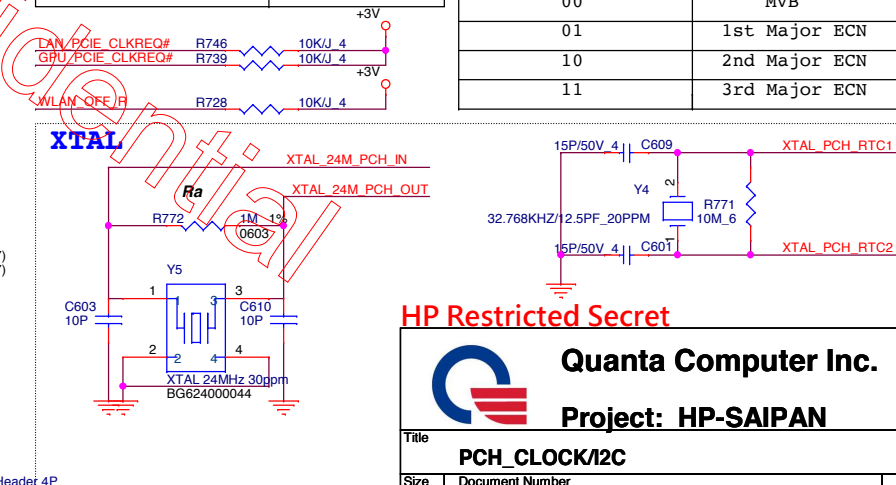








Board Rev[1:0]	Consumer AIO
00	All DB
01	All SI
10	PV1
11	PV2
00	MVB
01	1st Major ECN
10	2nd Major ECN
11	3rd Major ECN



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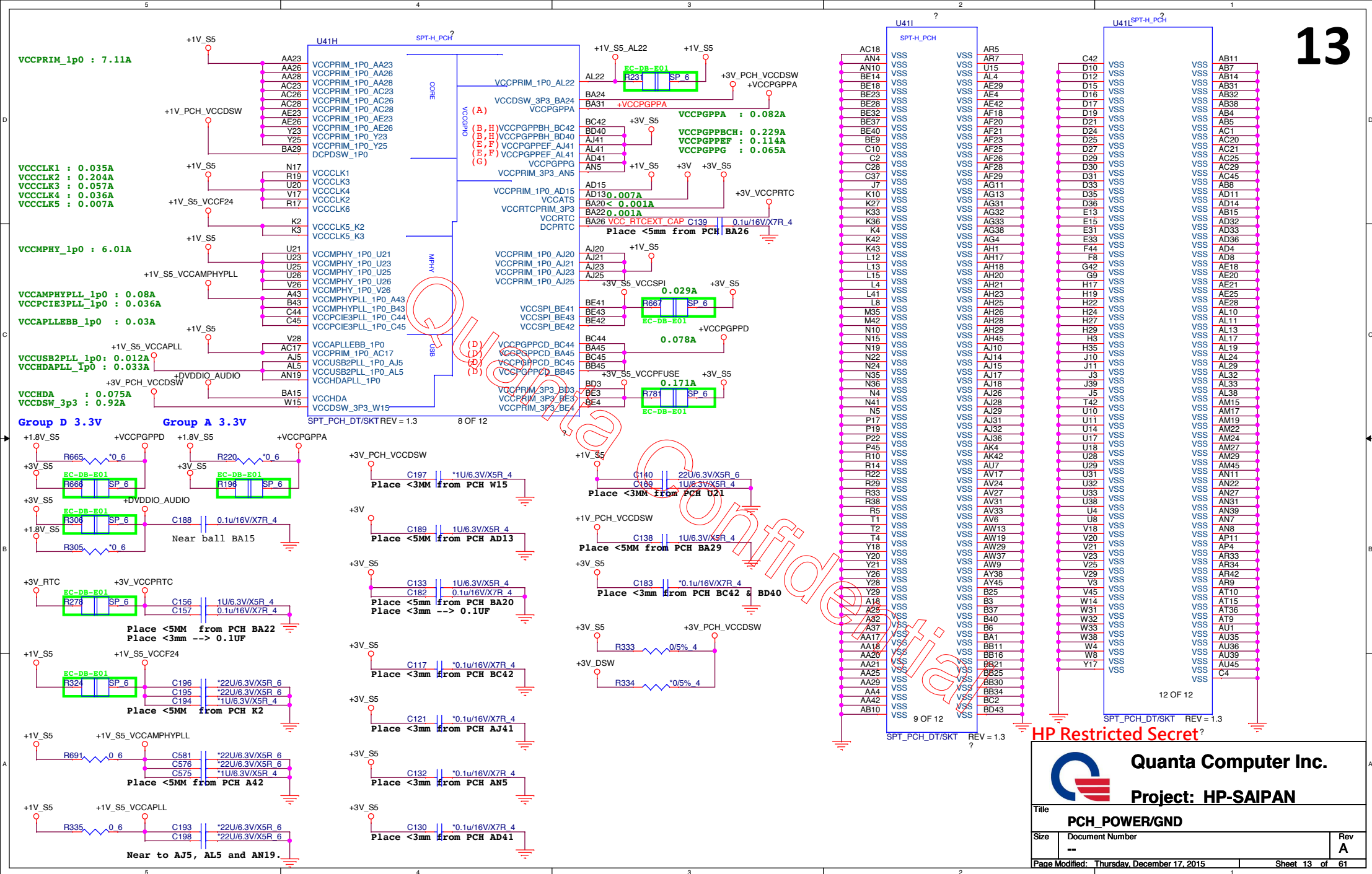
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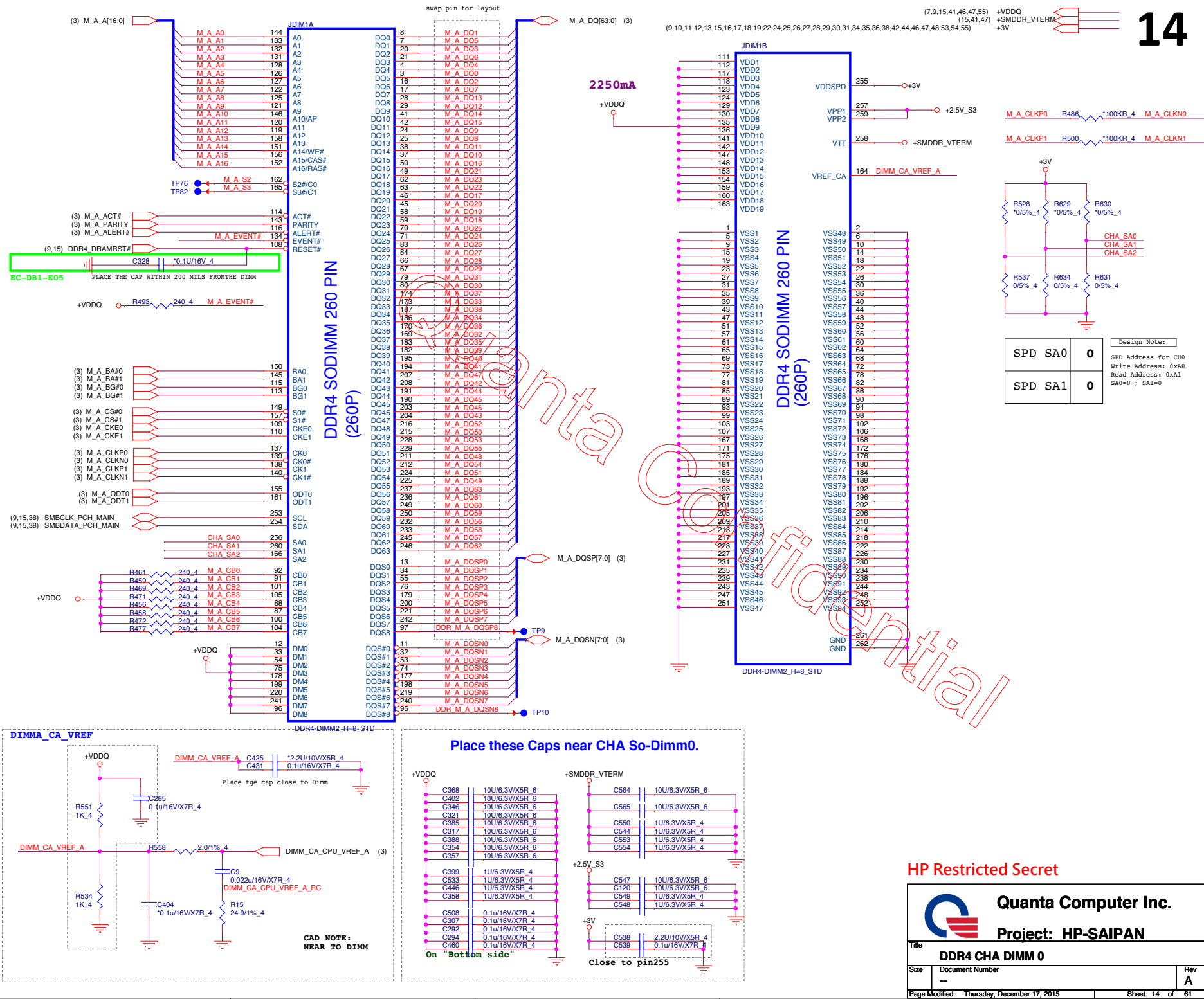
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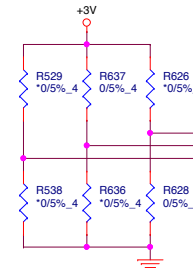
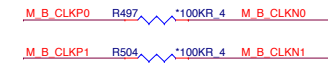
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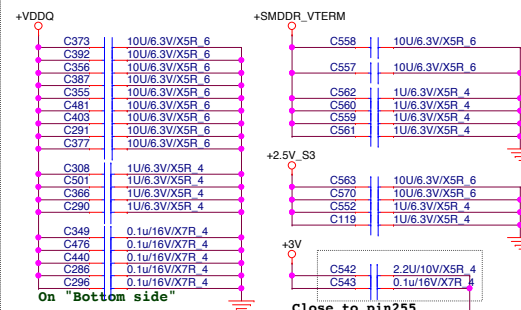








SPD SA0	0
SPD SA1	1



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Title  
**DDR4 CHB DIMM 1**

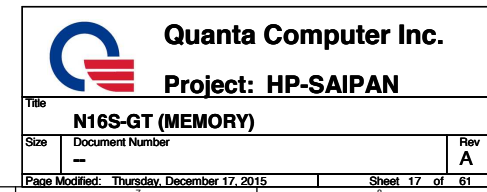
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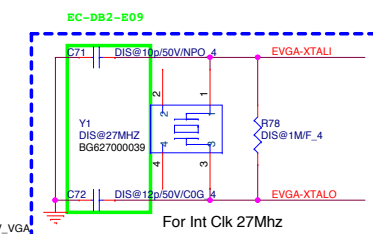
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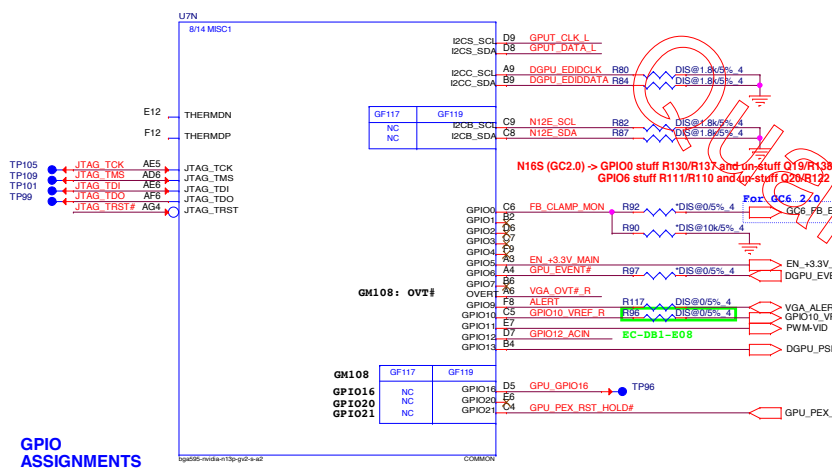
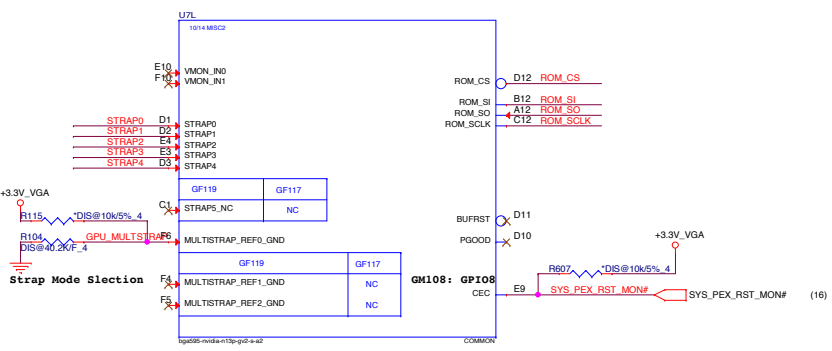
Sheet 15 of 61

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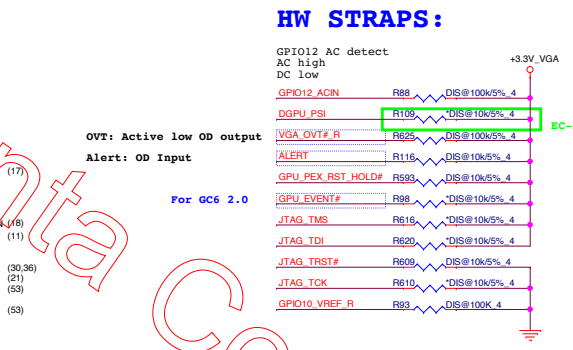
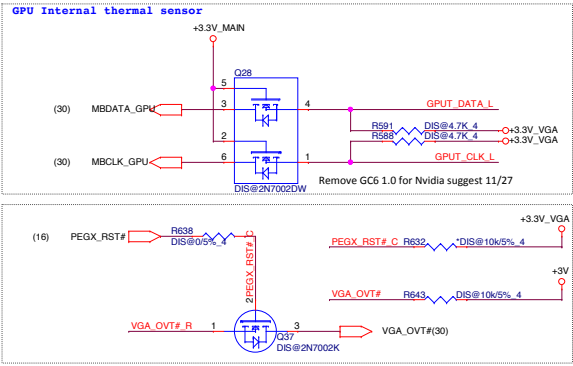




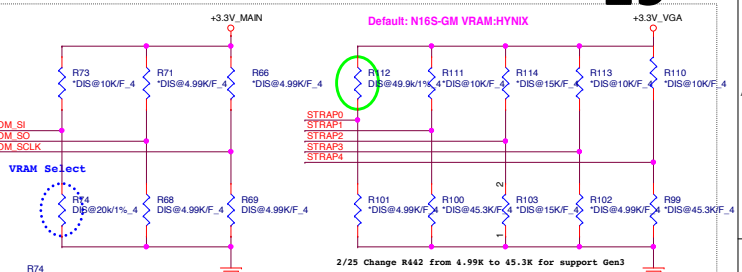




GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding



N16S-GM/GT-LP VRAM Configuration Table				ROM_SI			
RAMCFG [3:0]	DESCRIPTION	1.35V_gDDR5	Vendor	Vendor P/N	ROM_SI (R74)	STIN B/S	Configuration
0000	512Mx16		SAMSUNG	K4G80325FB-HC03	PD 4.99K ohm		
0001	256Mx16		Micron	MT51J256M32HF-60:A	PD 10K ohm		
0011			SAMSUNG	K4G41325FC-HC03	PD 20K ohm		
0110			HYNIX	H5GC424AJR-T2C	PD 34.8K ohm		

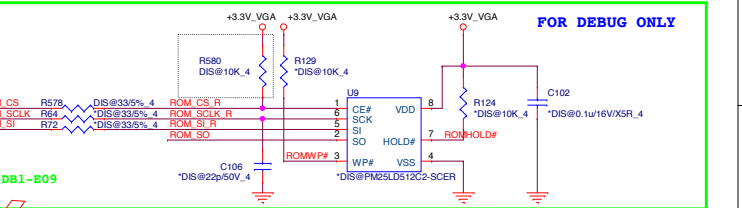


### N16S-GMR DID=0x134E

ROM\_SCLK = Stuff 4.99K PD  
ROM\_SI = Stuff 20K PD  
(VRAM Configuration follow below table)  
ROM\_SO = Stuff 4.99K PD  
STRAP0 = Stuff 49.9K PU  
STRAP1 = NC  
STRAP2 = NC  
STRAP3 = NC  
STRAP4 = NC

GB2B-64

Logical Strap Bit Mapping			
	PU-VDD	PD	QCI P/N
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB19
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB06
45.3K	1111	0111	CS34532FB18



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Project: HP-Saipan

Title: N16S-GT (GPIO/STRAPS)

Size: Document Number

Page Modified: Thursday, December 17, 2015

Sheet 19 of 61





**Project: HP-SAIPAN**

Rev
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A

Sheet 20 of 61



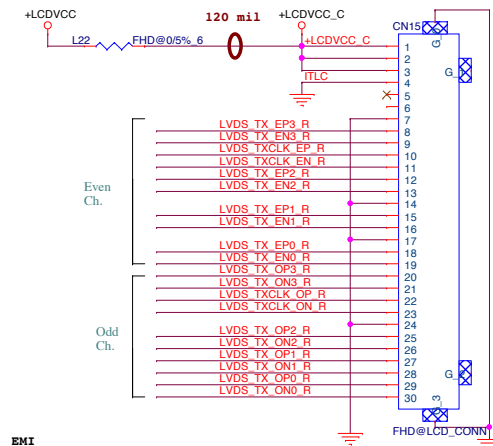




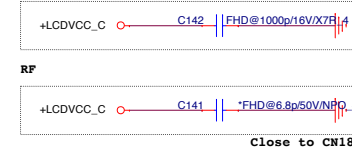
## 23



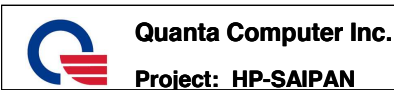
## LVDS Conn



## EMI

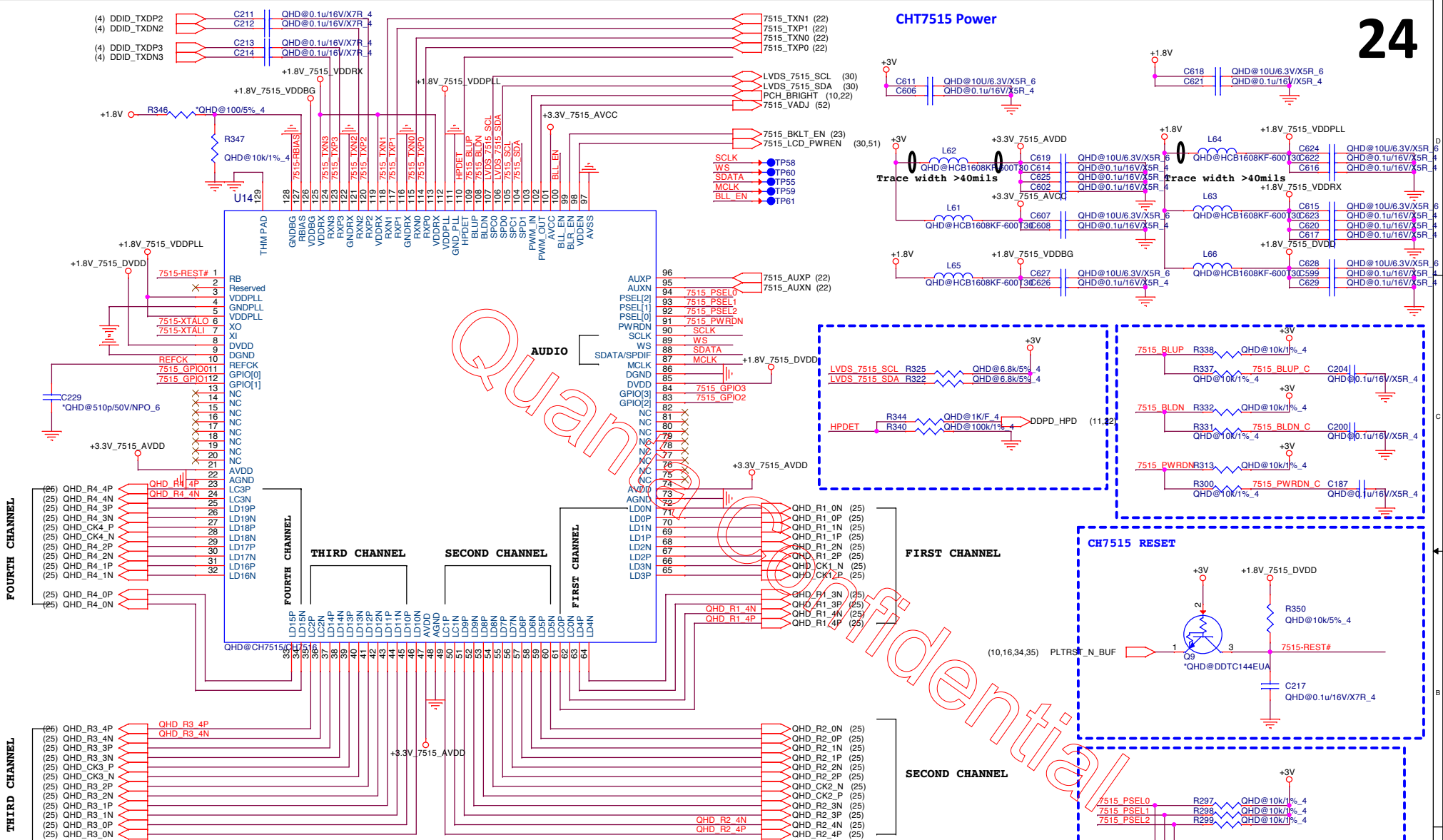


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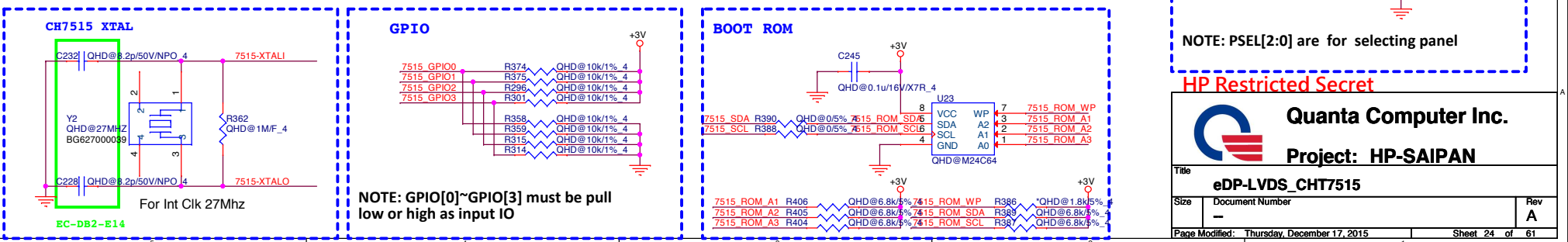


Title		Panel (Control).LCD-Conn.	
Size	Document Number		Revision
	---		A
Page Modified: Thursday, December 17, 2015		Sheet 23 of 61	

# CHT7515 Power



Note: It is an option that Each 100ohm resistor should be linked in each LVDS N/P differential signals



NOTE: PSEL[2:0] are for selecting panel

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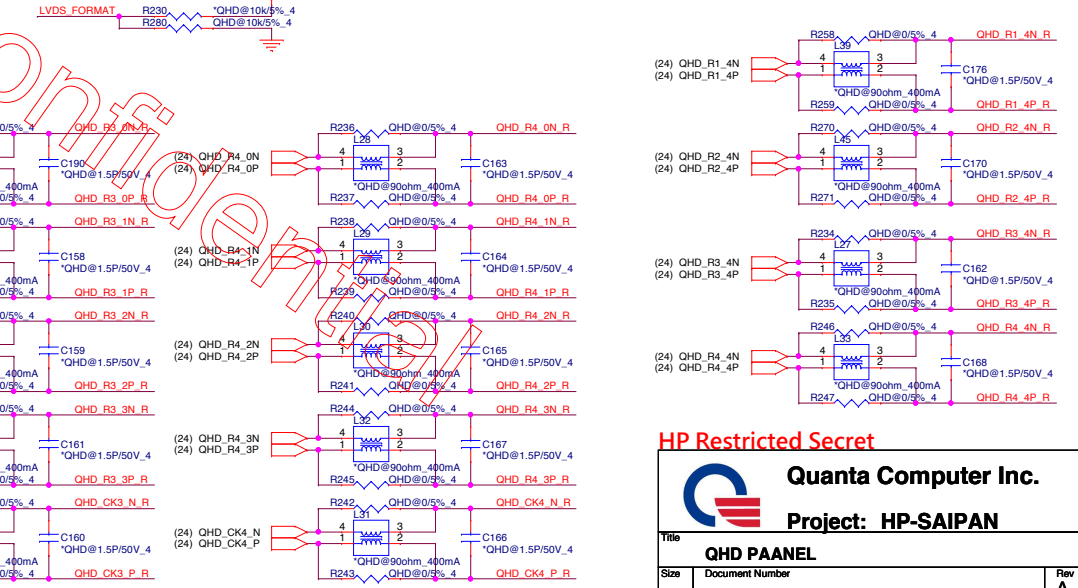
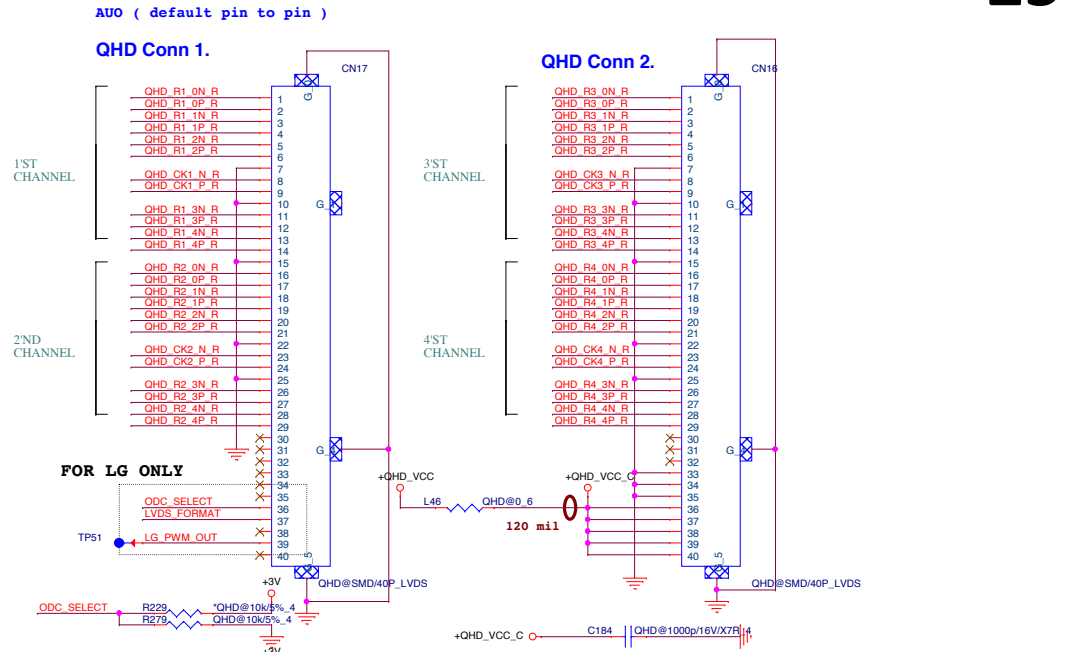
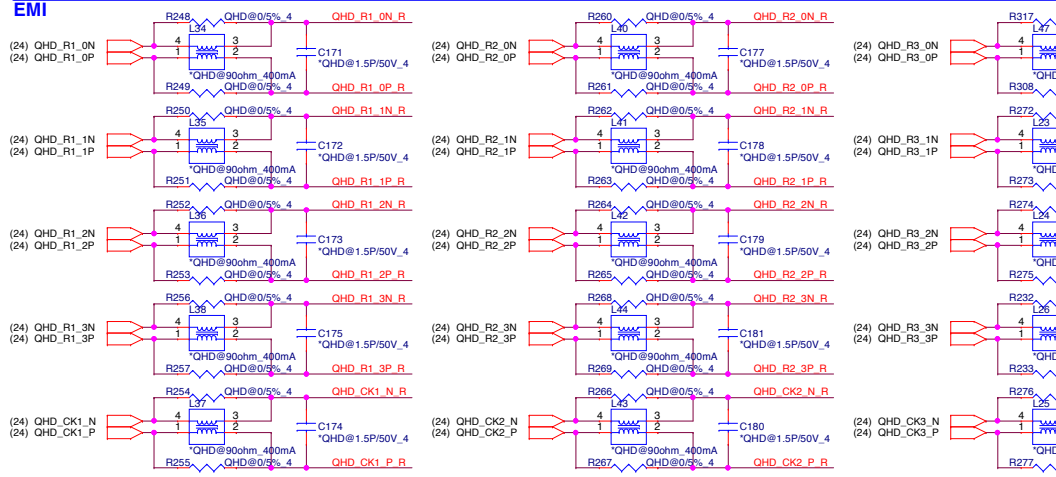
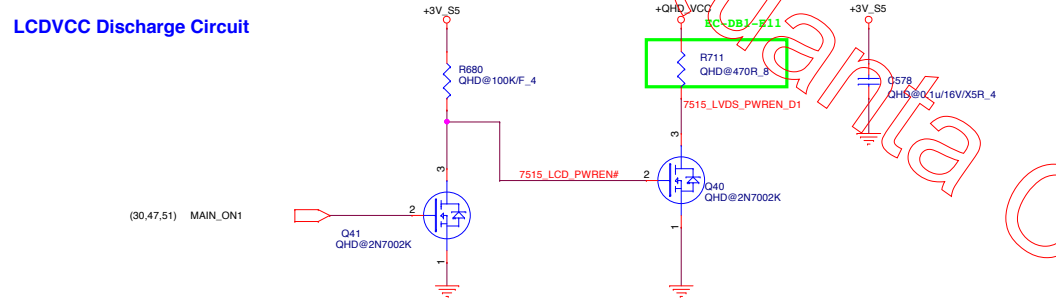
**Quanta Computer Inc.**

**Project: HP-SAIPAN**

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Size	Document Number	Rev	
		A	
Page Modified	Thursday, December 17, 2015	Sheet	24 of 61

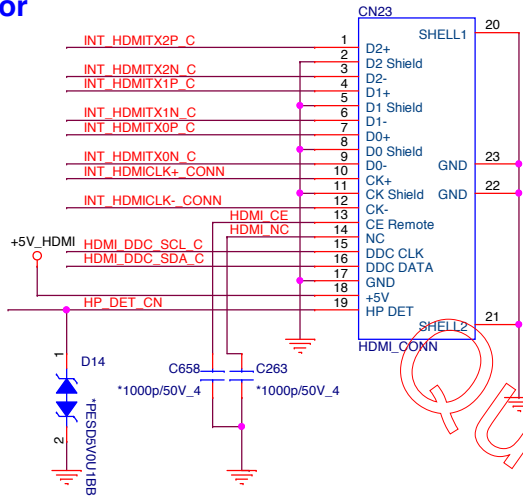
## LED PANEL

### PANEL VCC CONTROL

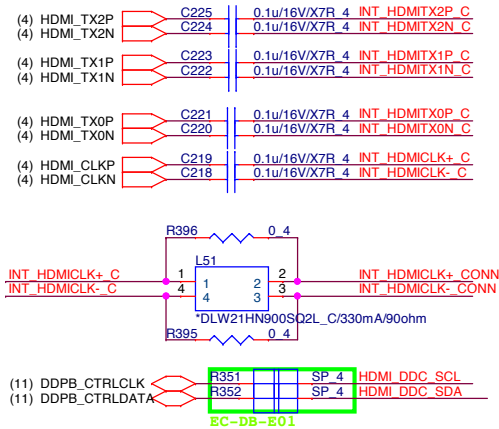




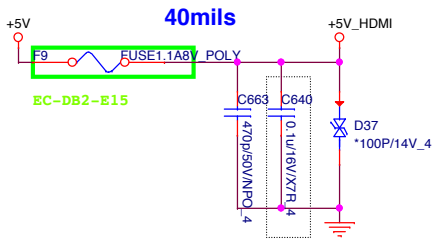
HDMI connector



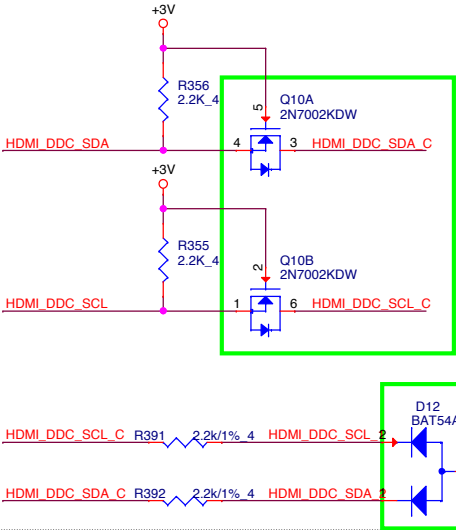
HDMI INTERFACE



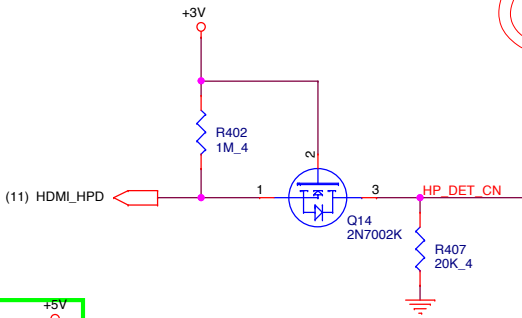
HDMI POWER SUPPLY



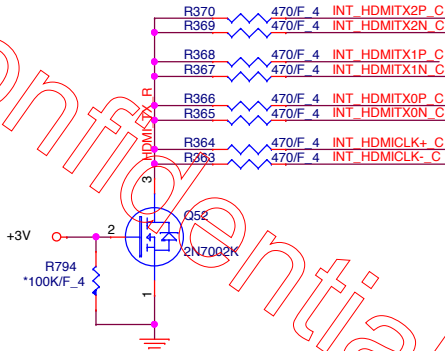
HDMI DDC



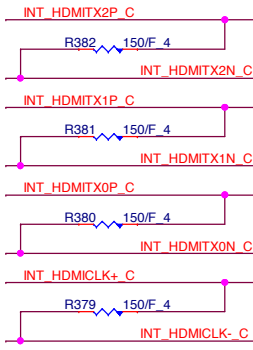
HDMI-detect



HDMI LEVEL SHIFT

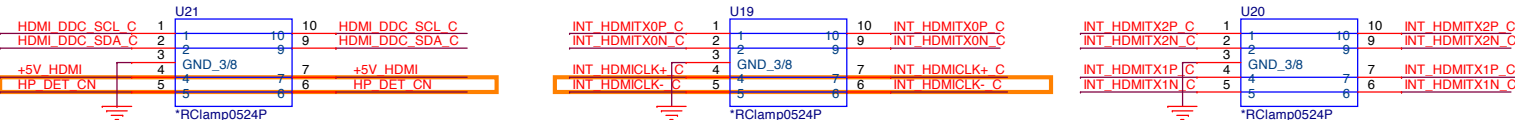


HDMI EMI (EMC)



ESD reserve for HDMI

Layout Notes:  
Place decoupling CAPs close to Connector



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**Project: HP-SAIPAN**

Title: **HDMI**

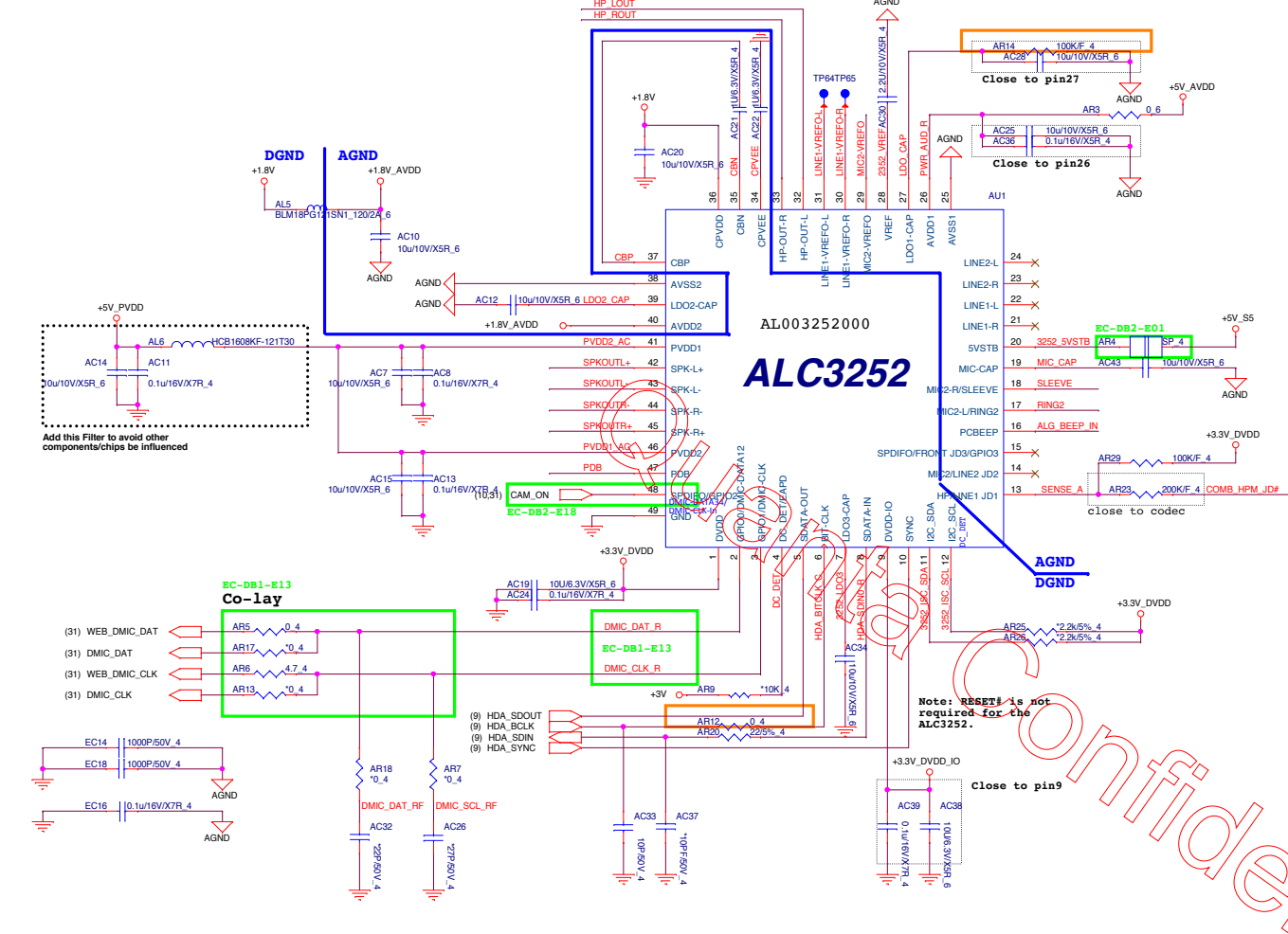
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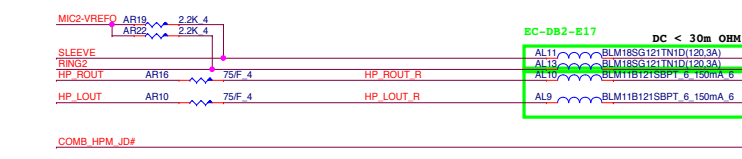
Rev: **A**

Sheet 26 of 61

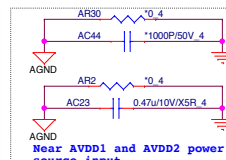
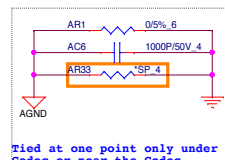




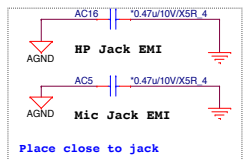
HeadPhone/Mic Combo Conn



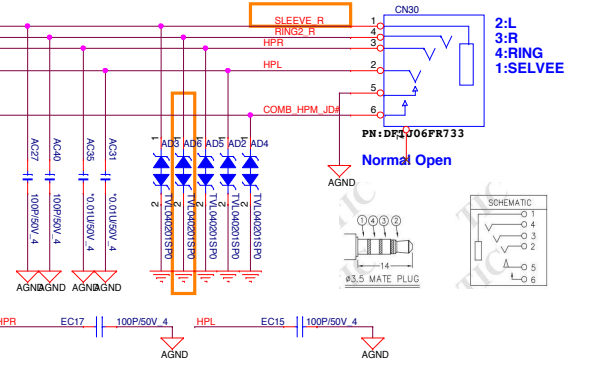
CODEC Return Path



EMI



PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.



27

(5,9,10,11,12,13,23,25,28,30,32,34,37,38,39,41,42,43,45,46,47,54,55)  
(9,10,11,12,13,14,15,16,17,18,19,22,24,25,26,28,29,30,31,34,35,36,38,42,44,46,47,48,53,54,55)

+5V  
+3V\_S5  
+3V

### AUDIO AVDD POWER

DGND plane AGND plane

Moat

In order to prevent the built-in LDO damaged from over-voltage on +5V\_S5 or Standby power line, we suggested using this Voltage suppressing device.

### AUDIO DVDD/DVDD\_IO POWER

AL8, AL12, AL17, AL18, AC17, AC18, AC42, AC41

### AUDIO PVDD POWER

Normally DC-DET pin is low level to turn on Power Switch(Q5)  
When DC is detected from Class D output, DC-DET pin is floating to turn off Power Switch(Q5)

### EC MUTE

EC\_MUTE#

### PCBEEP

SPKR

### Internal Speaker (2W, 4 ohm)

SPKOUTL, SPKOUTR, INT\_R\_SPK+, INT\_L\_SPK+, INT\_R\_SPK-, INT\_L\_SPK-

Change Connector: DFHD04MR424  
FP: 50291-00401-v01-4p-1dv\_ab

Pin	Signal
A1	B1 INT_R_SPK+
A2	B2 INT_R_SPK-
A3	B3 INT_L_SPK+
A4	B4 INT_L_SPK-

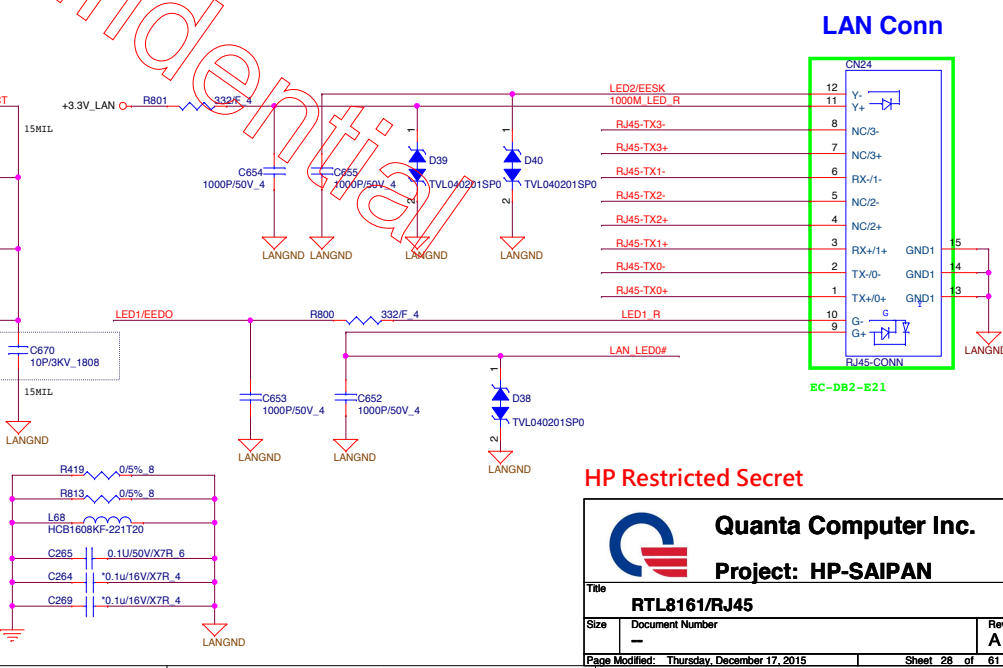
**Quanta Computer Inc.**

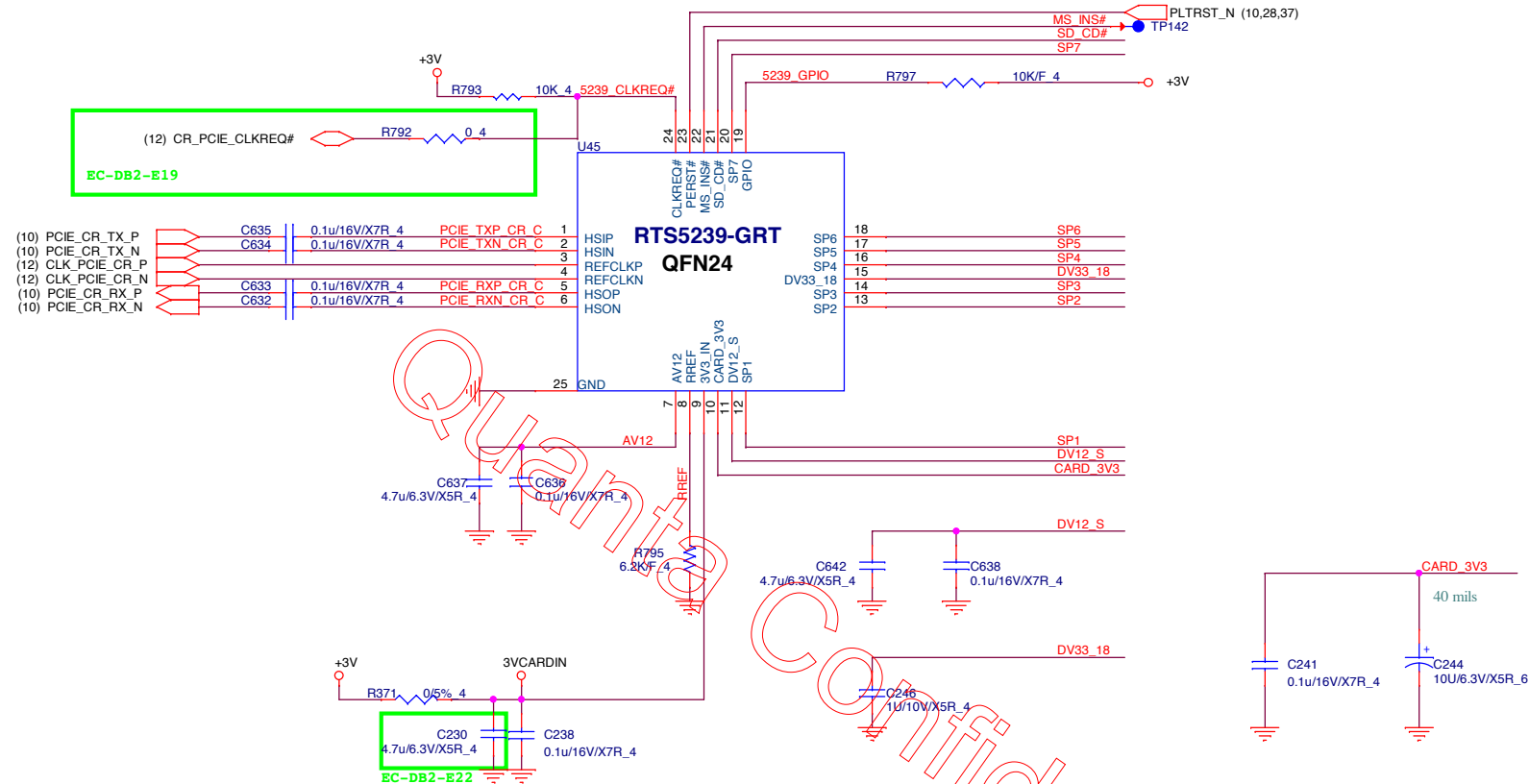
**Project: HP-Saipan**

**Audio ALC3228-CG**

Title	Size	Document Number	Rev
			A

Page Modified: Thursday, December 17, 2015 Sheet 27 of 61





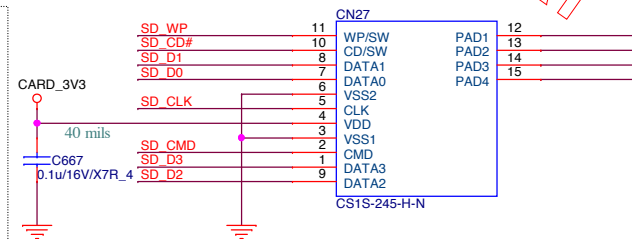
## EMI EC-DB2-E23

SD_D1	C664	*5.6P/16V_4
SD_D0	C665	*5.6P/16V_4
SD_CLK	C666	4.7P/50V_4
SD_D3	C668	*5.6P/16V_4
SD_D2	C669	*5.6P/16V_4

## SD damping resistor

SP1	R805	33 4	SD_D1
SP2	R806	33 4	SD_D0
SP3	R807	33 4	SD_CLK
SP4	R810	33 4	SD_CMD
SP5	R808	33 4	SD_D3
SP6	R809	33 4	SD_D2
SP7	R796	33 4	SD_WP

## SD connector



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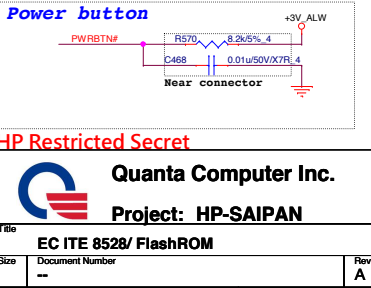
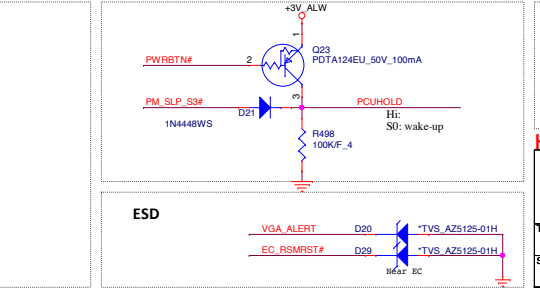
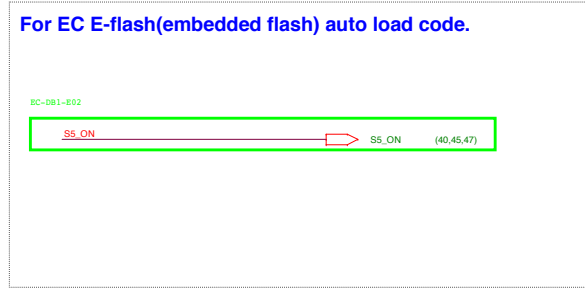
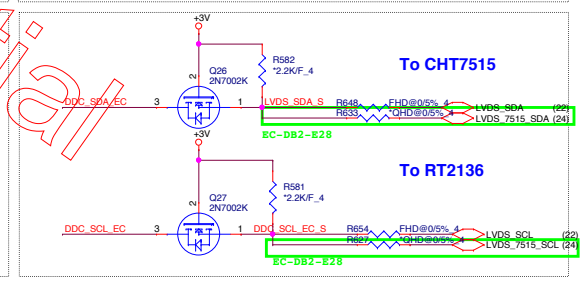
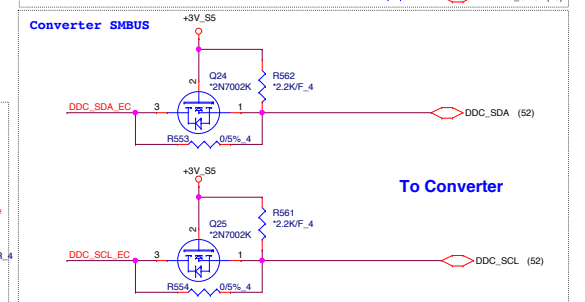
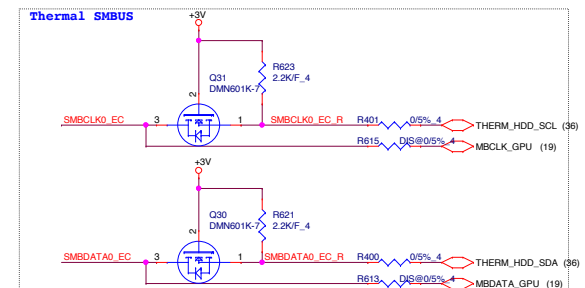
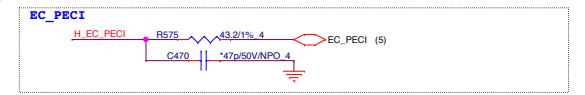
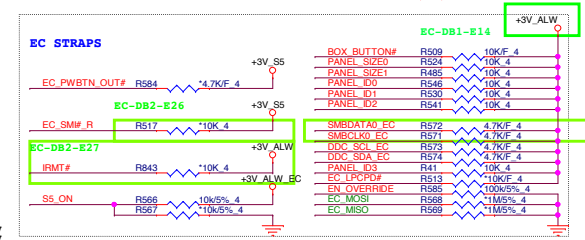
Quanta Computer Inc.

Project: HP-SAIPAN

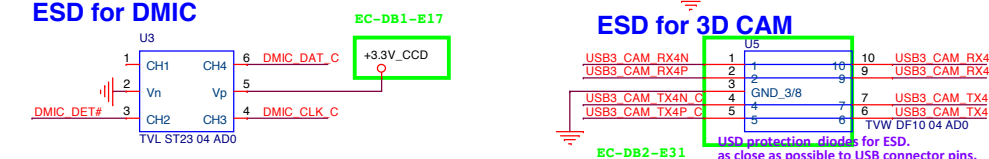
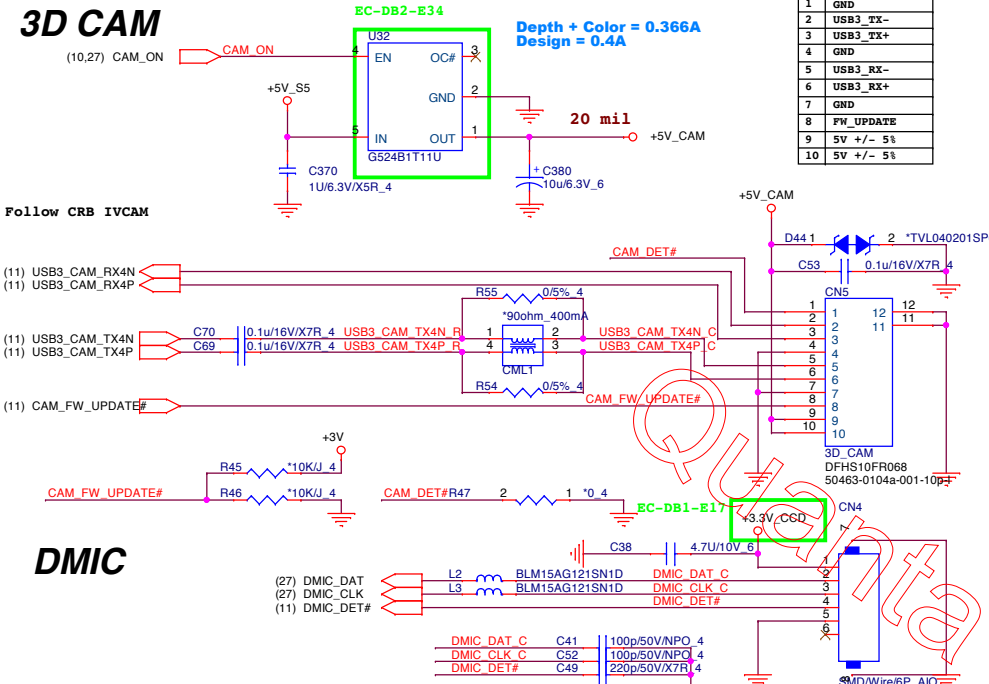
Title  
Card Reader (RTS5239)Size  
Document Number  
Rev  
A

Page Modified: Thursday, December 17, 2015

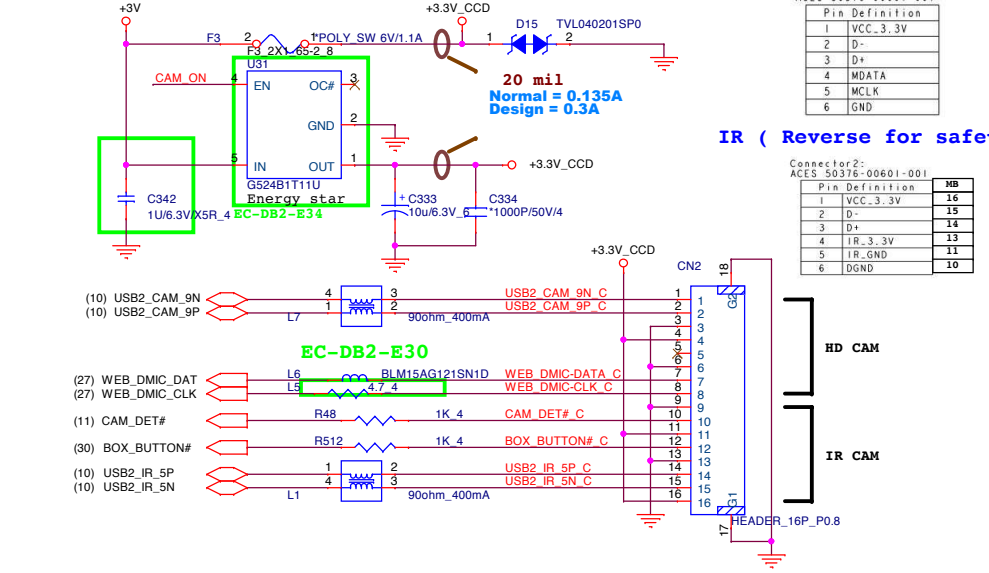
Sheet 29 of 61



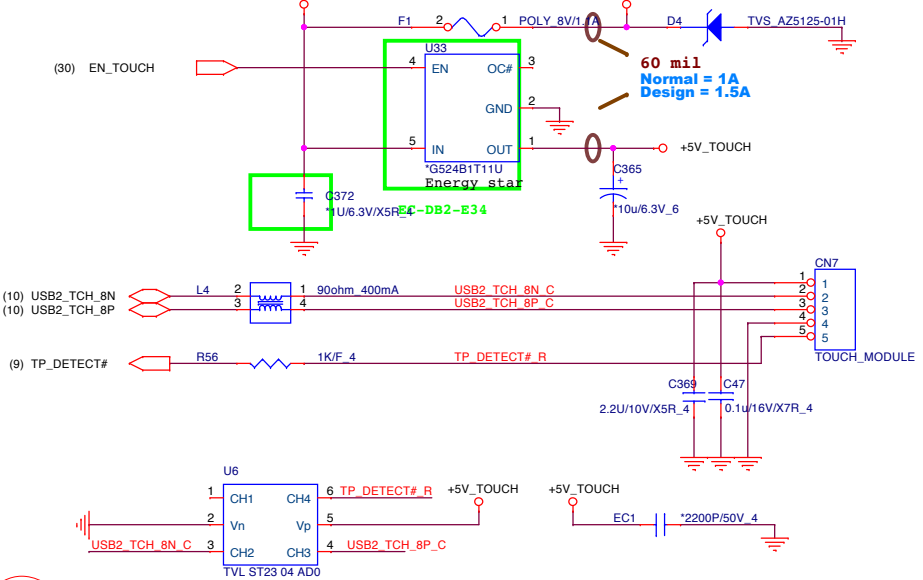
(Optional 1: 3DCAM+DMIC)



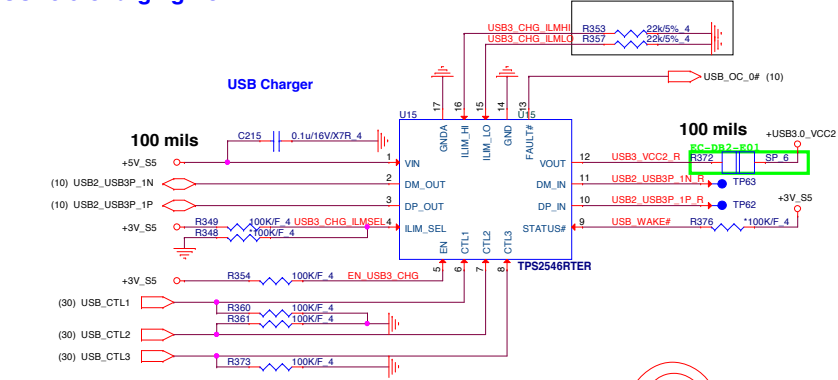
(Optional 2: WEBCAM+DMIC)



Touch Panel

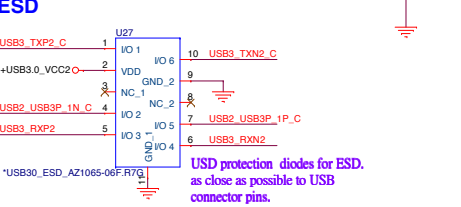
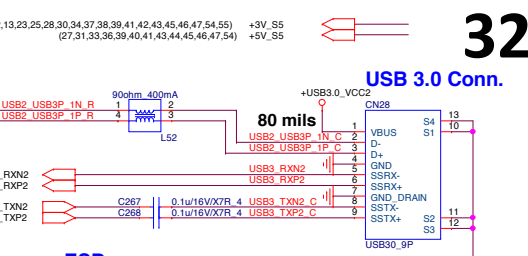


USB PORT  
USB3.0 Charging Port

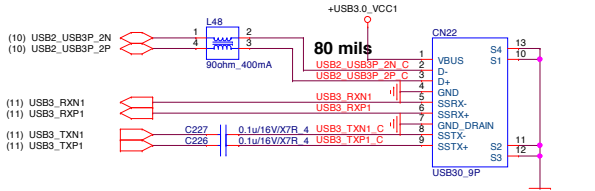
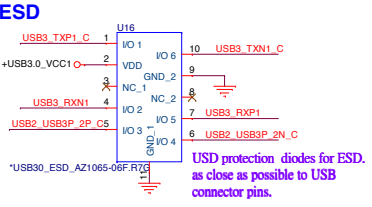
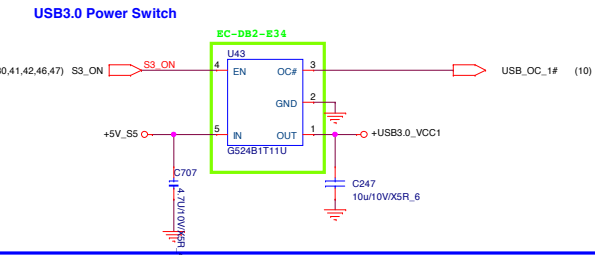


SDP : Standard Downstream Port  
CDP : Charging downstream port  
DCP : Dedicated Charging Port  
Enable/Disable : setting by BIOS

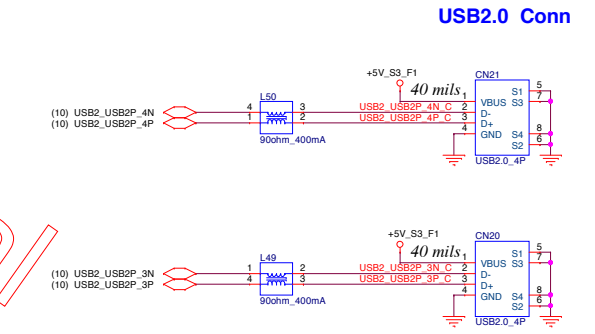
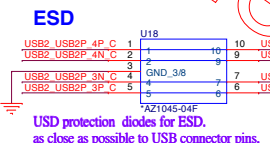
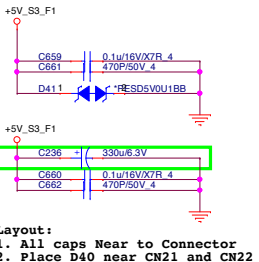
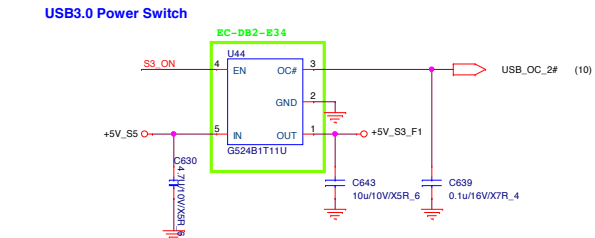
POWER STATE	TPS2546 CHARGING MODE	CTRL1	CTRL2	CTRL3	ILIM
S0	CDP LOAD DETECTION WITH ILIM_LO +60MA THRESHOLDS OR IF A BC1.2 PRIMARY DETECTION OCCURS	1	1	1	1
S3	AUTO MODE, LOAD DETECTION WITH POWER WAKE THRESHOLDS	0	1	1	1
S4/S5	AUTO MODE, KEYBOARD/ MOUSE WAKE-UP, LOAD DETECTION WITH ILIM_LO +60MA THRESHOLDS	0	0	1	1



USB3.0 PORT

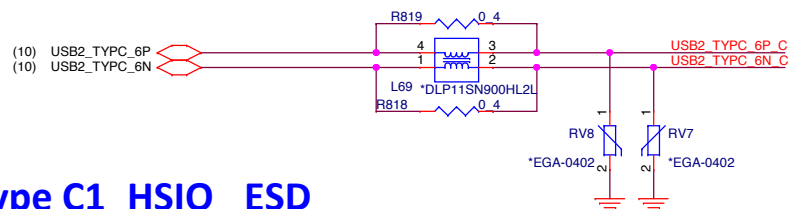


USB2.0 X 2

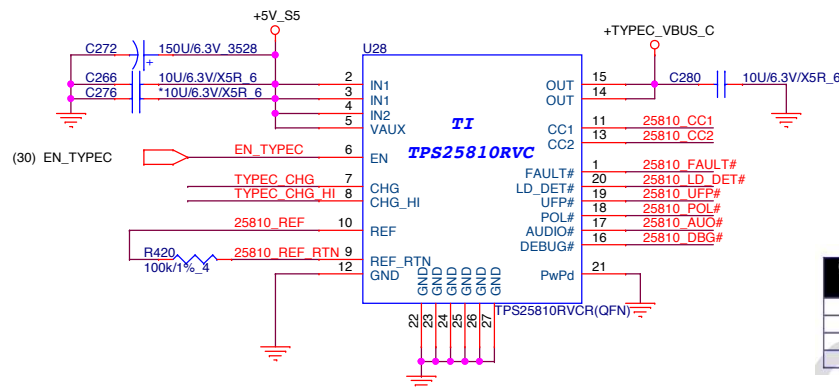
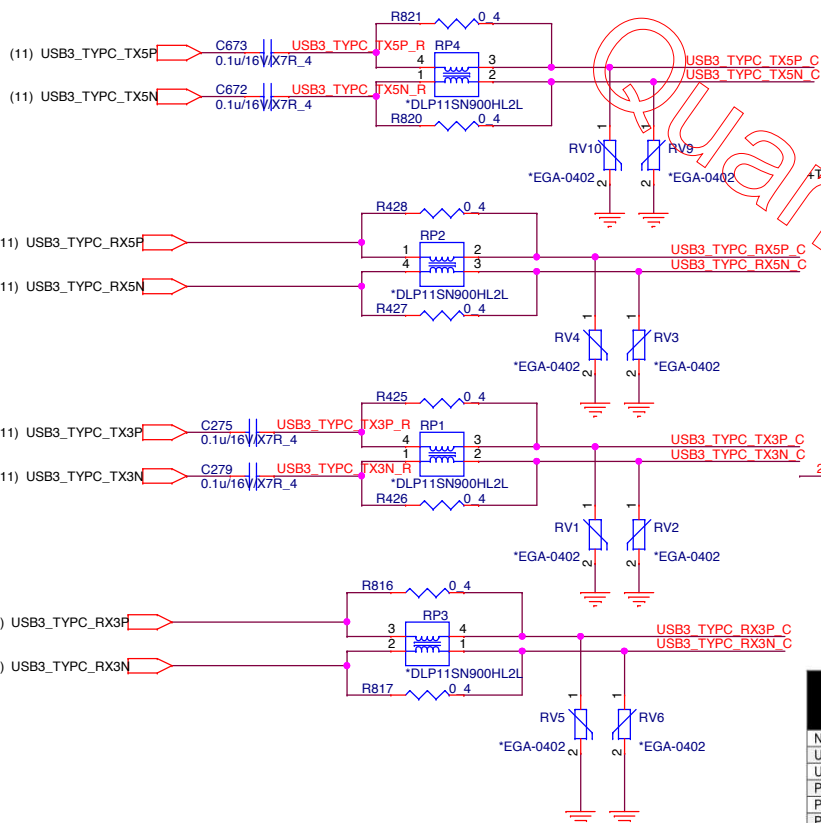




## USB2.0 ESD



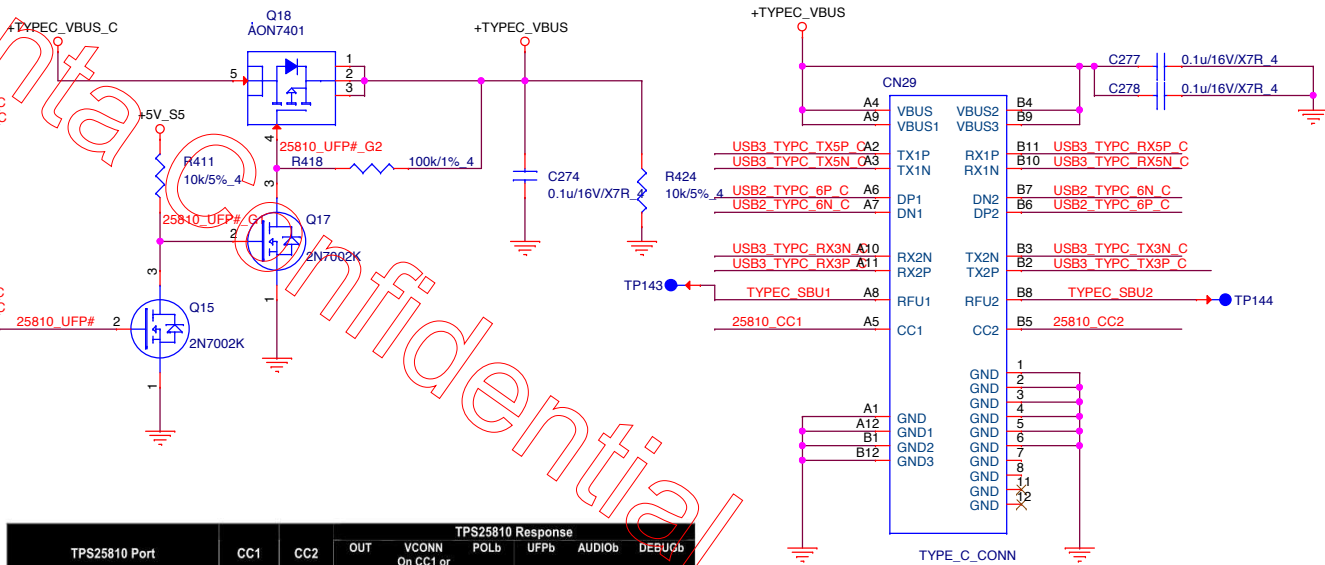
## Type C1\_HSIO\_ESD



25810_FAULT#	R434	100K/F	4
25810_LD_DET#	R433	100K/F	4
25810_UFP#	R432	100K/F	4
25810_POL#	R431	100K/F	4
25810_AUDIO#	R430	100K/F	4
25810_DBG#	R429	100K/F	4

TYPEC_CHG	R415	100K/F	4
TYPEC_CHG_HI	R414	100K/F	4

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A



TPS25810 Port	CC1	CC2	OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

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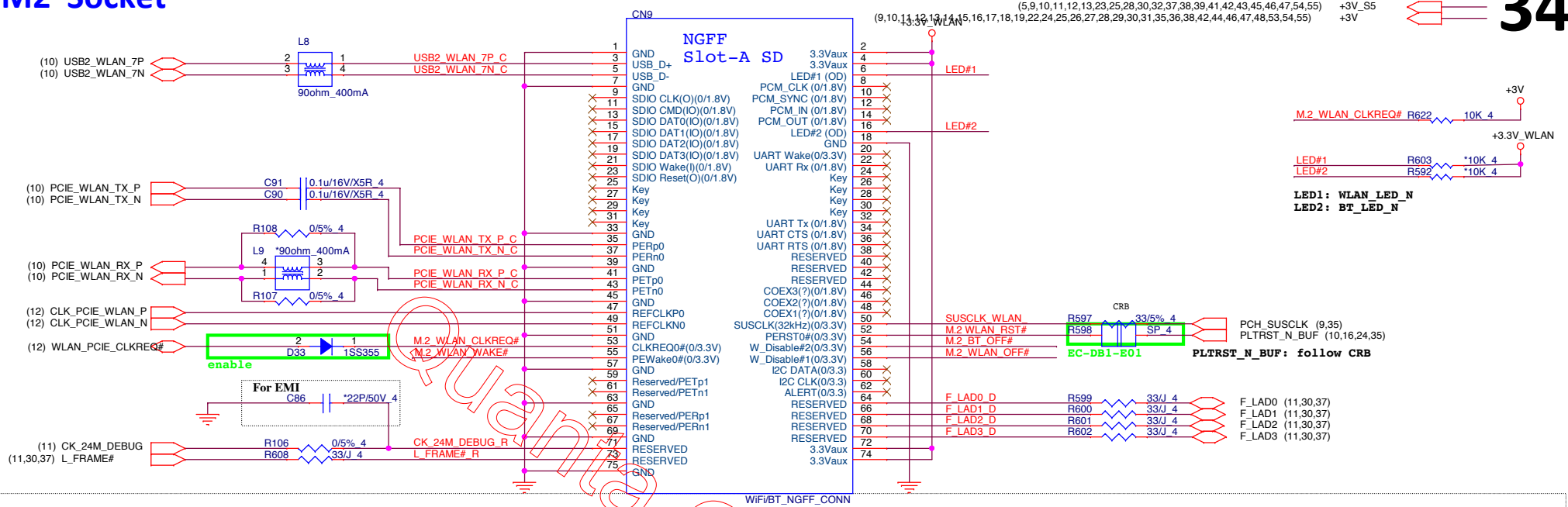
Project: HP-SAIPAN

Title	USB TYPE-C		
Size	Document Number	Rev A	
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Page Modified:	Thursday, December 17, 2015	Sheet 33 of 61	

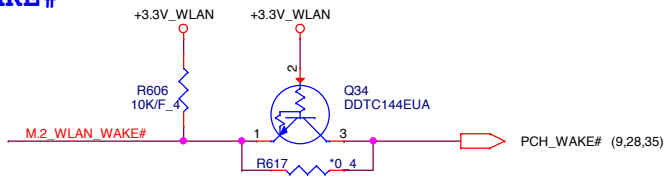
## NGFF M2 Socket

H=9.0

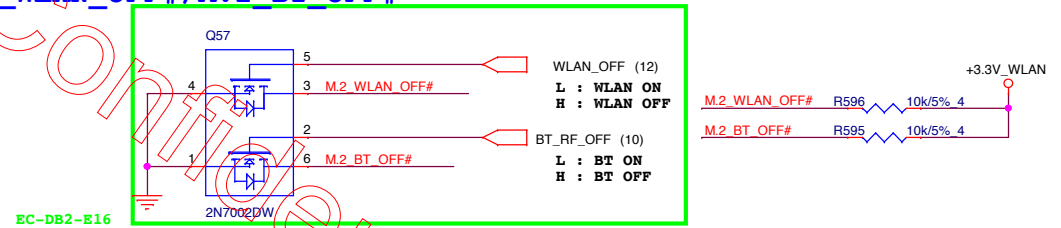
# 34



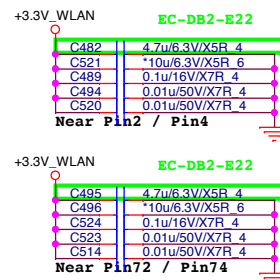
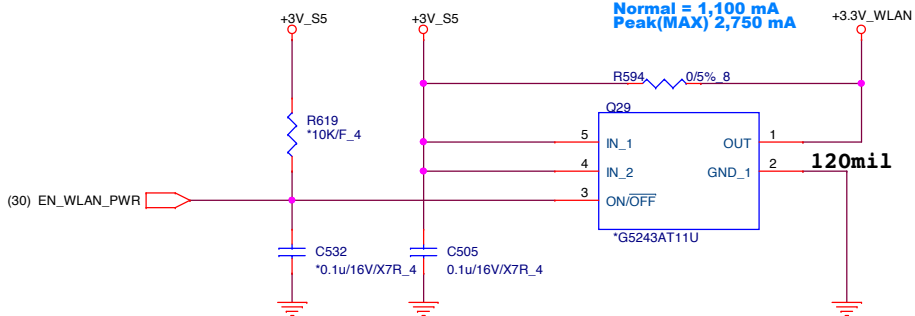
## M.2 WLAN WAKE#



**M.2\_WLAN\_OFF#/M.2\_BT\_OFF#**



## NGFF M2\_power(S5)



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**Quanta Computer Inc.****Project: HP-SAIPAN**

Title **NGFF M.2 WLAN**

Size	Document Number
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Rev  
B

Page Modified: Thursday, December 17, 2015

Sheet 34 of 61

# NGFF M2 Socket

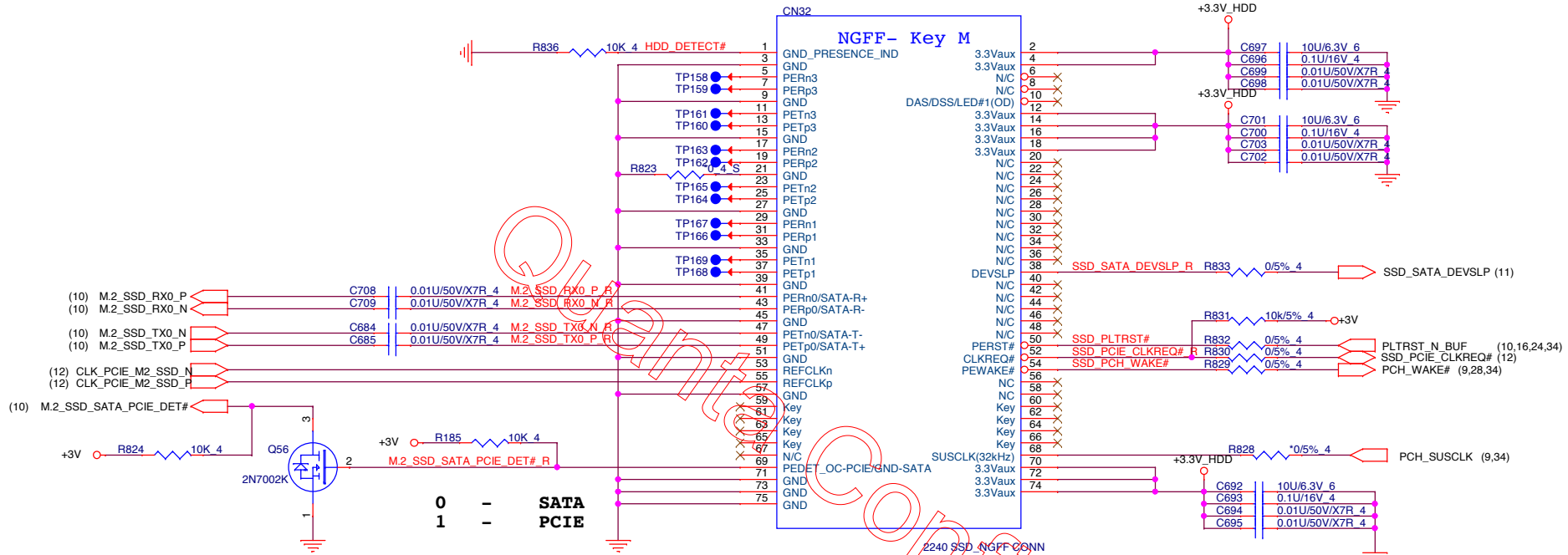
(5,9,10,11,12,13,23,25,28,30,32,34,37,38,39,41,42,43,45,46,47,54,55) +3V\_S5  
(9,10,11,12,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30,31,34,36,38,42,44,46,47,48,53,54,55) +3V

35

60 mil 1.5A

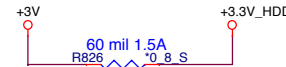
EC-DB2-E36

H=9.0



For Skylake platforms, need to implement the polarity inversion on the board using a NOT gate IC so that PCH will correctly interpret the interface detect signaling from the M.2 device.

DC Current rating: 3 A (MAX)



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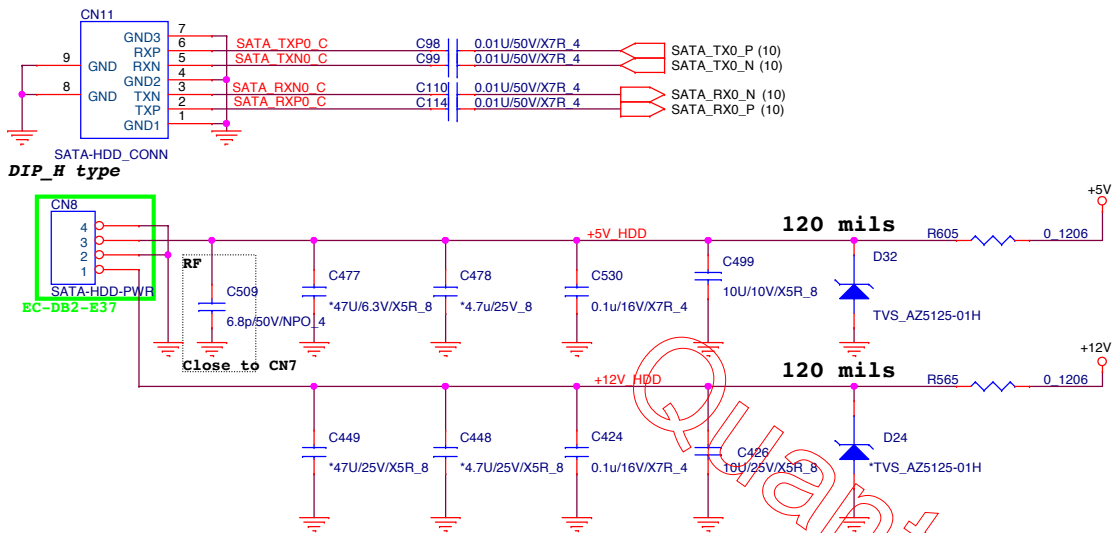


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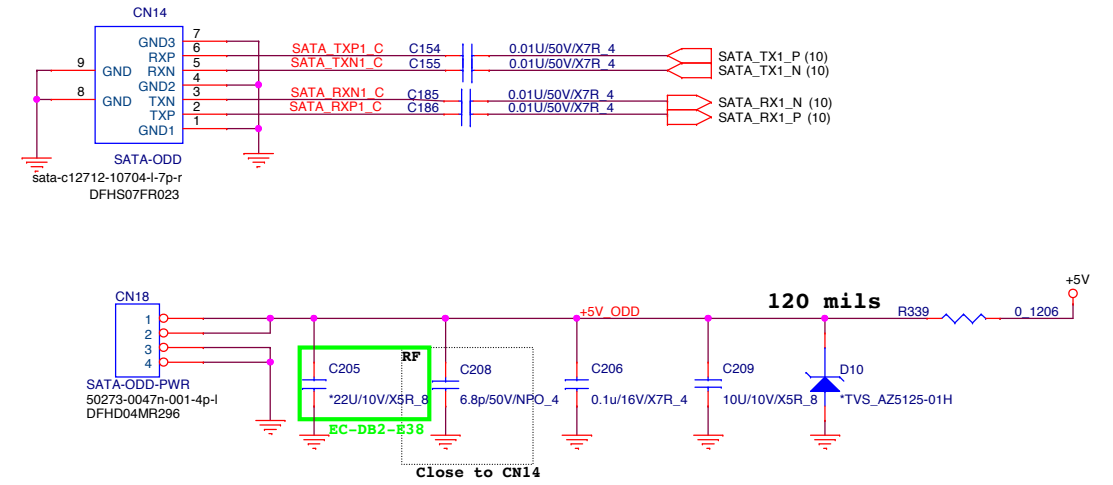
Project: HP-Saipan

Title <b>NGFF M.2 WLAN</b>		
Size	Document Number	Rev <b>B</b>
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Page Modified: Thursday, December 17, 2015		Sheet 35 of 61

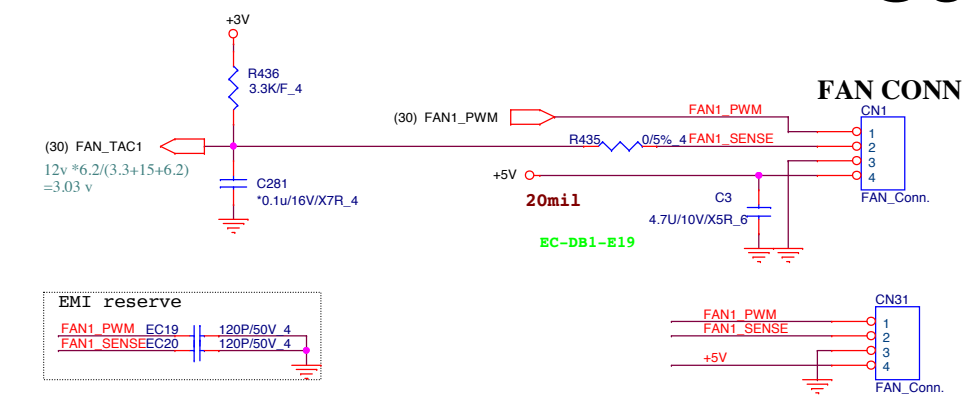
SATA HDD  
HDD SATA Conn.



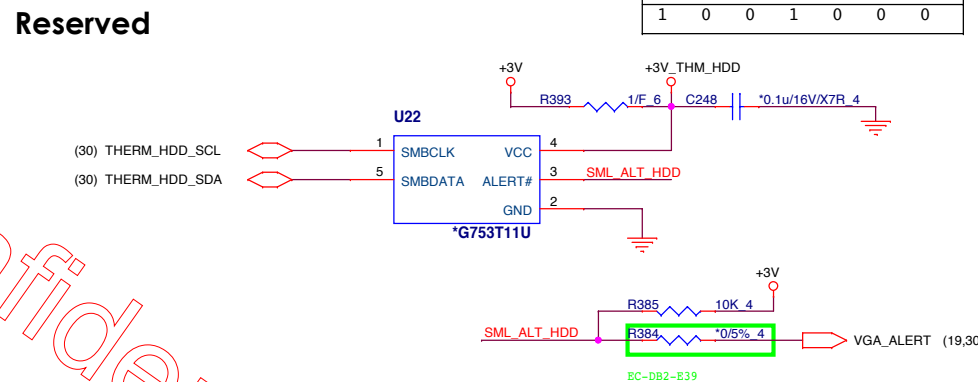
SATA ODD  
ODD SATA Conn.



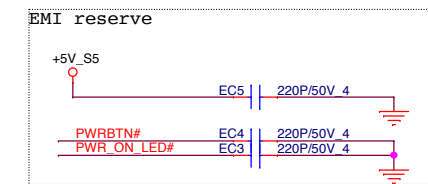
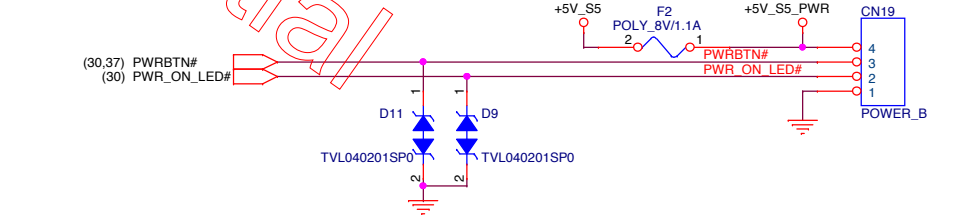
SYSTEM FAN




Ambient SENSOR



Power Button.



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**Project: HP-SAIPAN**

Title <b>FAN/HDD/ODD/HDD CONN.</b>		
Size	Document Number	Rev <b>A</b>
Page Modified: Thursday, December 17, 2015		Sheet 36 of 61

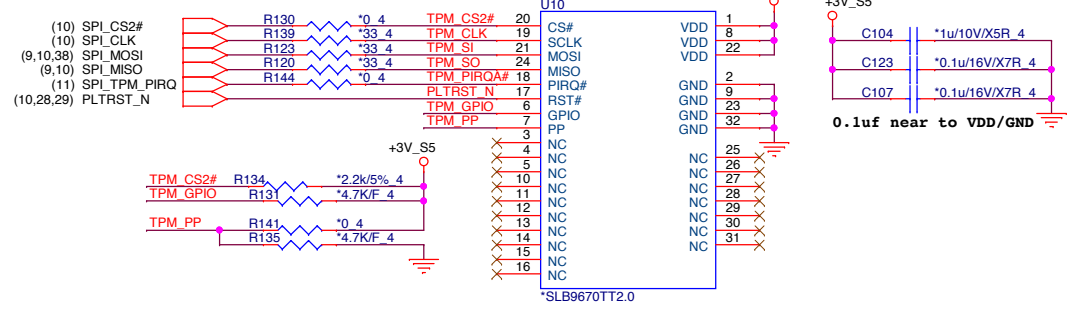
# TPM2.0

(5,9,10,11,12,13,23,25,28,30,32,34,38,39,41,42,43,45,46,47,54,55)  
(9,10,11,12,13,14,15,16,17,18,19,22,24,25,26,27,28,29,30,31,34,35,36,38,42,44,46,47,48,53,54,55)  
(23,26,27,31,36,39,46,47,48,49,50,53,55)  
(5,7,9,38,46,47,48)

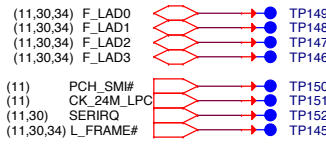


37

## SPI TPM2.0

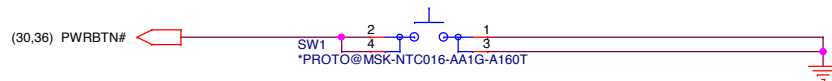


## LPC HEADER



EC-DB2-E40

SW1 For Debug.MP will remove it.



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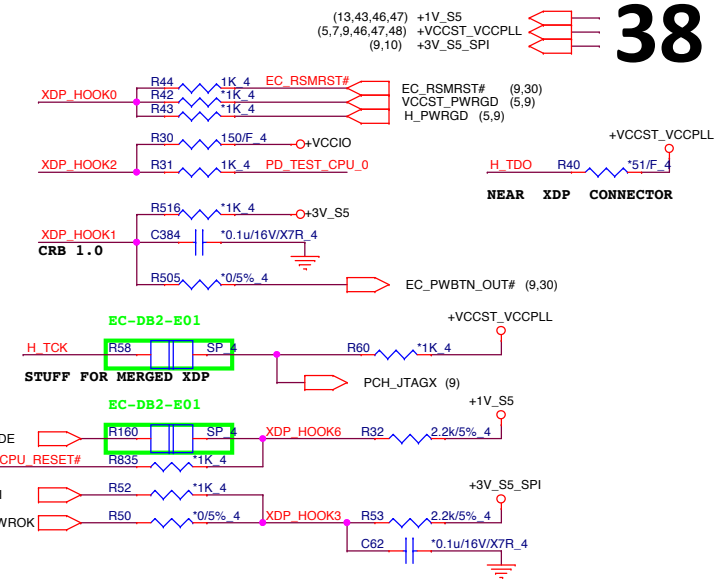
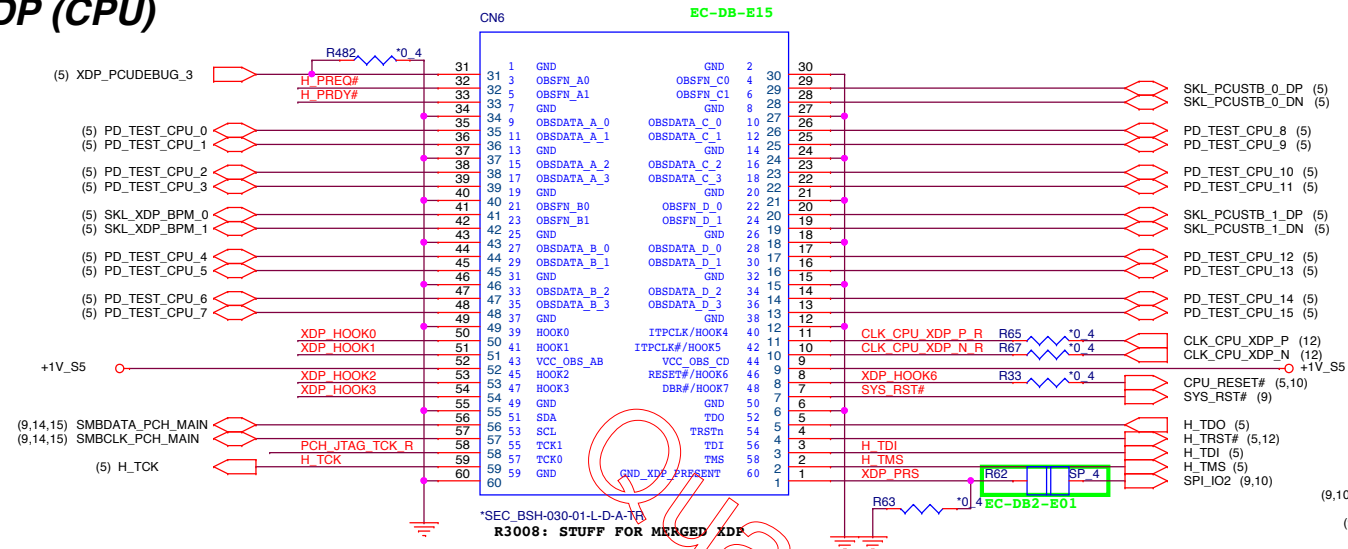
Project: HP-SAIPAN

Title	Debug /LPC Header/TPM		
Size	Document Number	Rev	A
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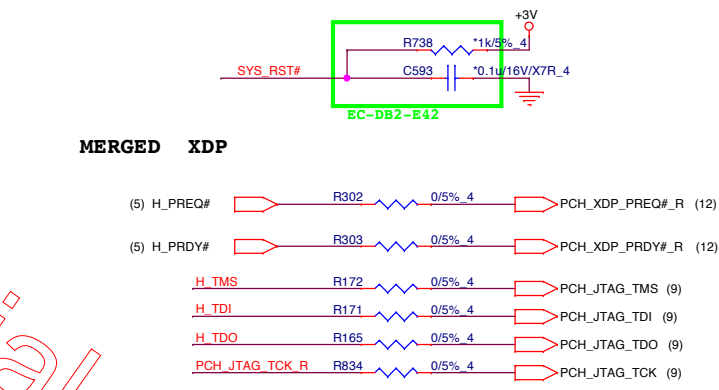
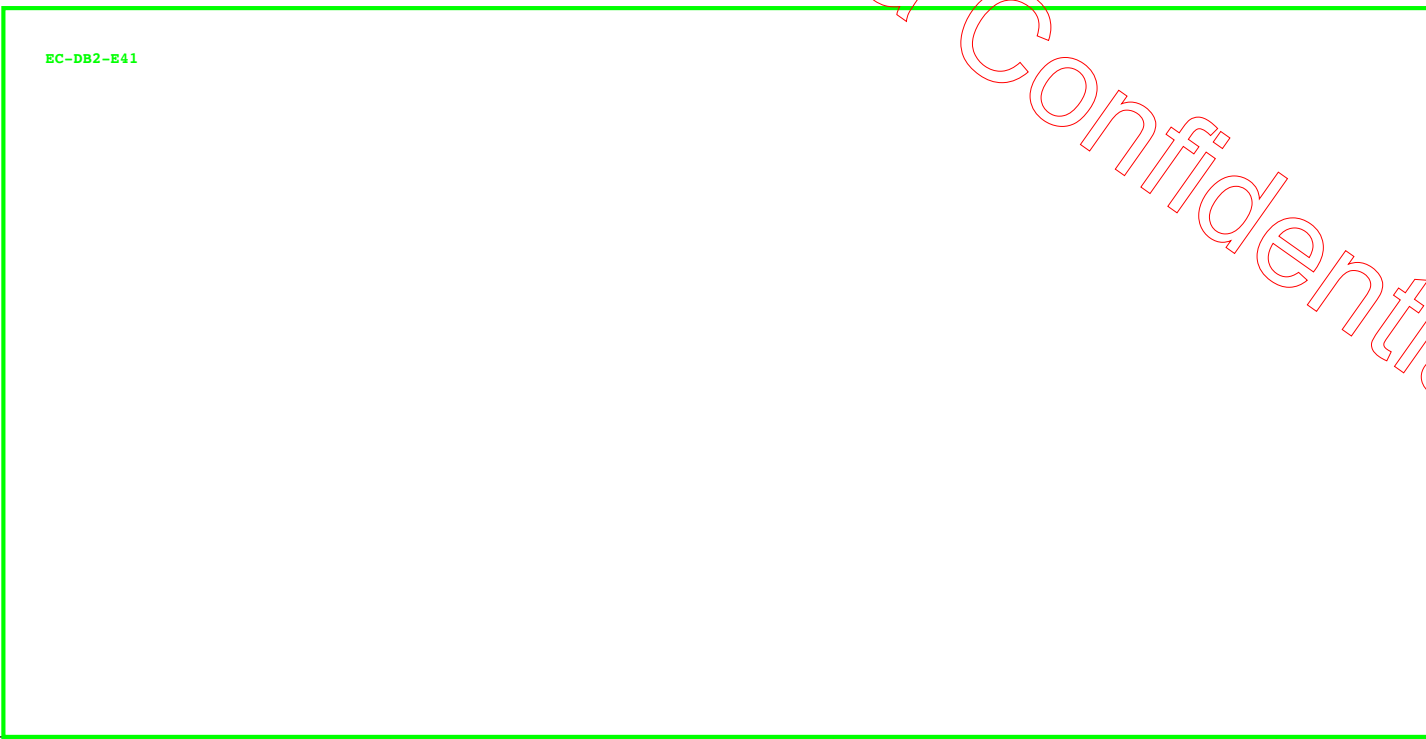
Page Modified: Thursday, December 17, 2015 Sheet 37 of 61



XDP (CPU)



XDP (PCH)



stuff for merged XDP

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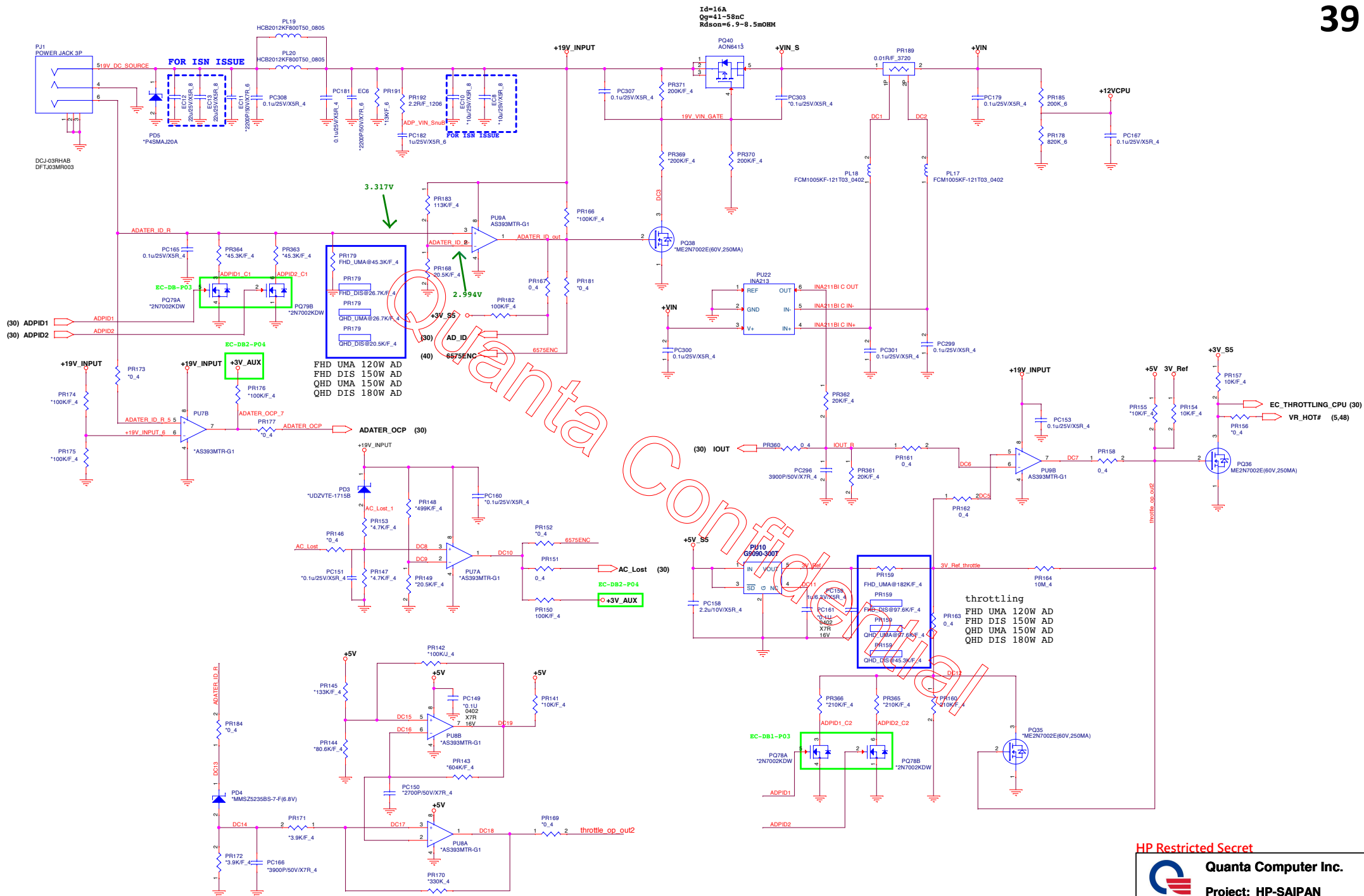
**Project: HP-Saipan**

**XDP DEBUG**

Size	Document Number	Rev
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Page Modified: Thursday, December 17, 2015

Sheet 38 of 61




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Project: HP-SAIPAN

 <b>Project: HP-Saipan</b>		
<b>Title</b> <b>DC-IN</b>		
<b>Size</b> --	<b>Document Number</b> --	<b>Rev</b> <b>A</b>
<b>Page Modified:</b> Thursday, December 17, 2015		<b>Sheet</b> 39 <b>of</b> 61



MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8065-H	DFN3x3	13A	14.5m
TPCA8A10-H	DFN5x6	40A	3.8m

### Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

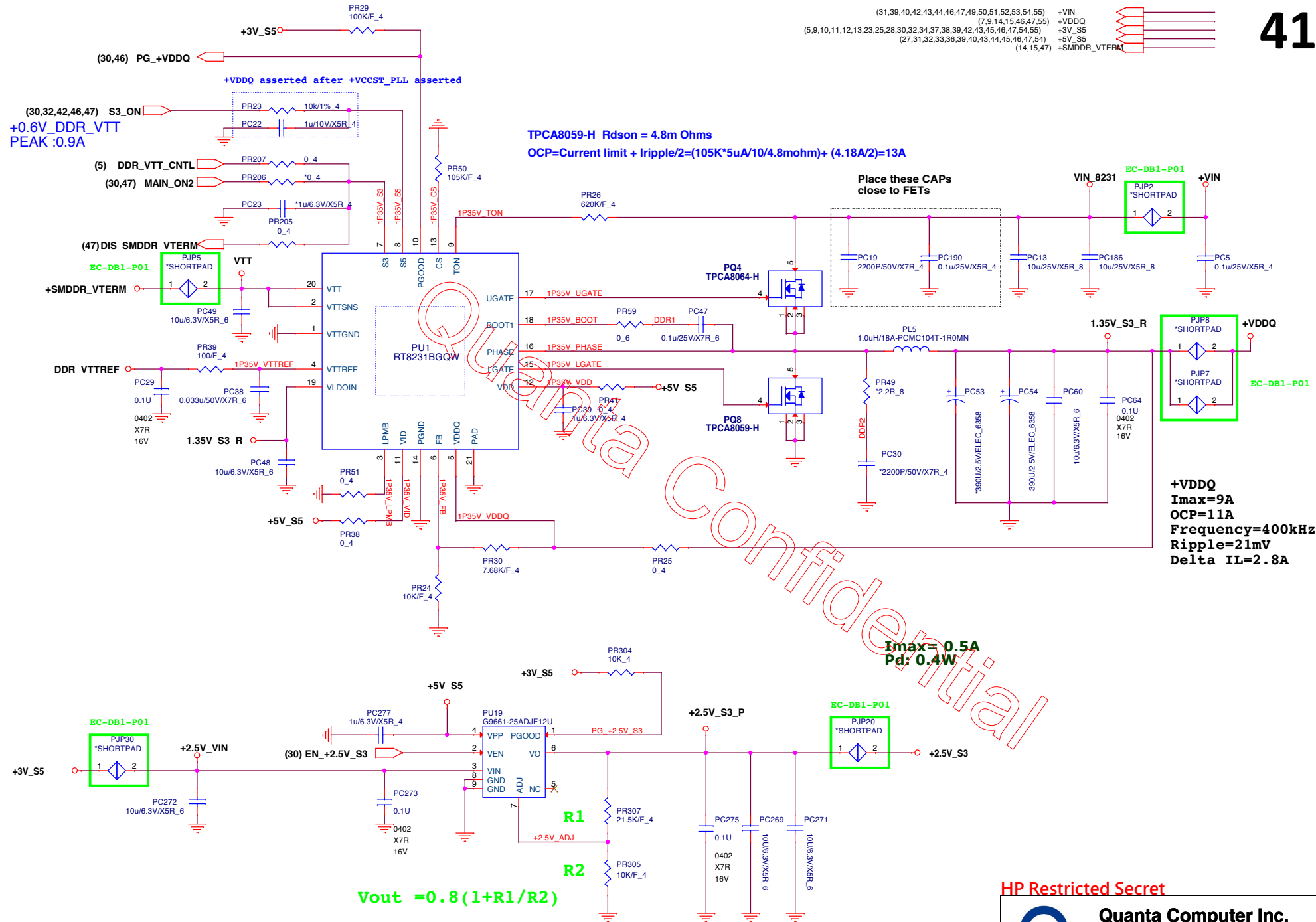
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**Quanta Computer Inc.****Project: HP-SAIPAN**

Title	3V AUX/5V S5(RT6575AGQW)
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Size	Document Number	Rev
	---	A
Page Modified: Thursday, December 17, 2015		Sheet 40 of 61

+0.6V\_DDR\_VTT  
PEAK :0.9A



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Quanta Computer Inc.

Project: HP-SAIPAN

Title: +VDDQ /SMDDR\_VTERM (RT8231BGQW)

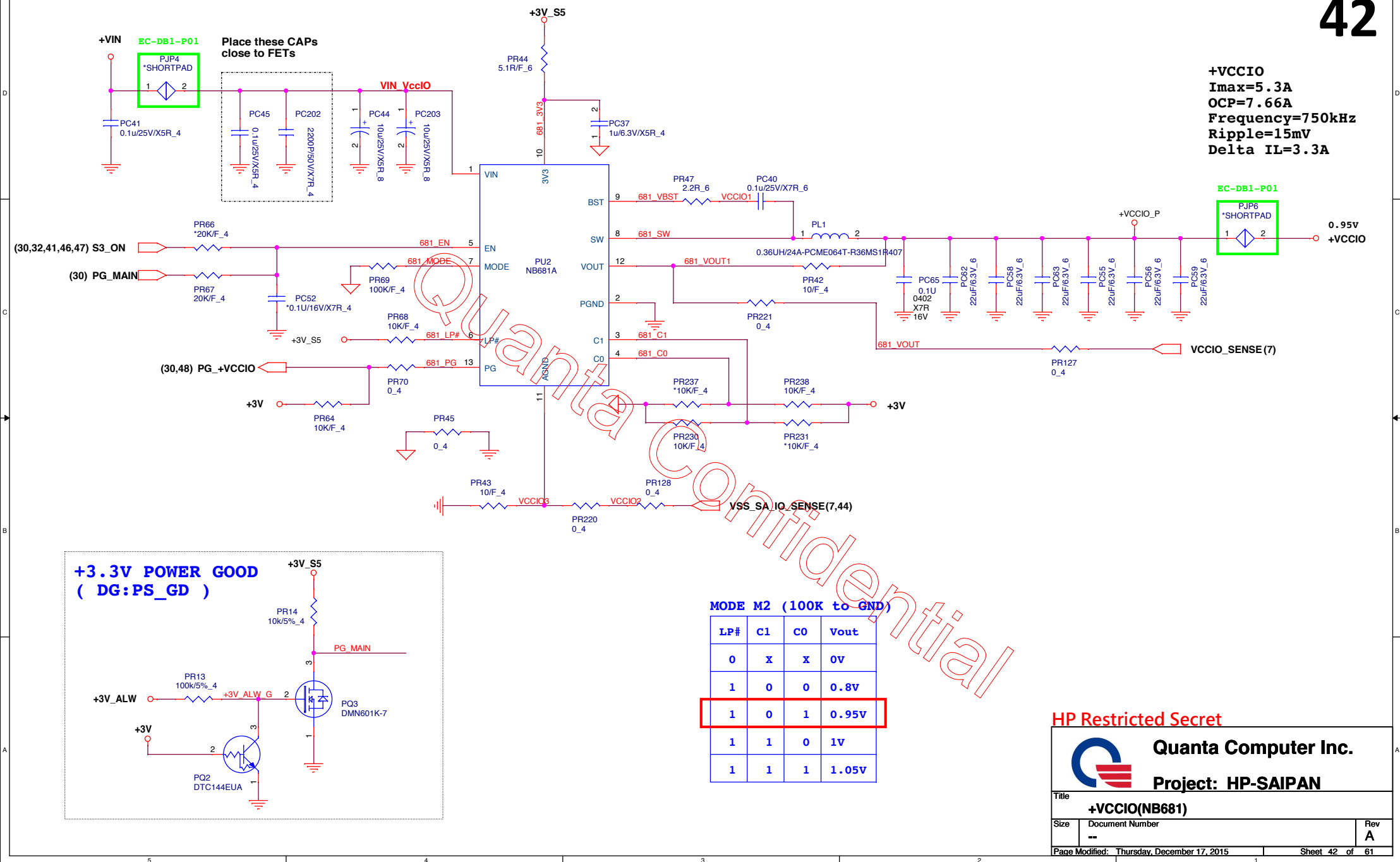
Size: Document Number

Rev

Page Modified:

Thursday, December 17, 2015

Sheet 41 of 61



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Project: HP-SAIPAN

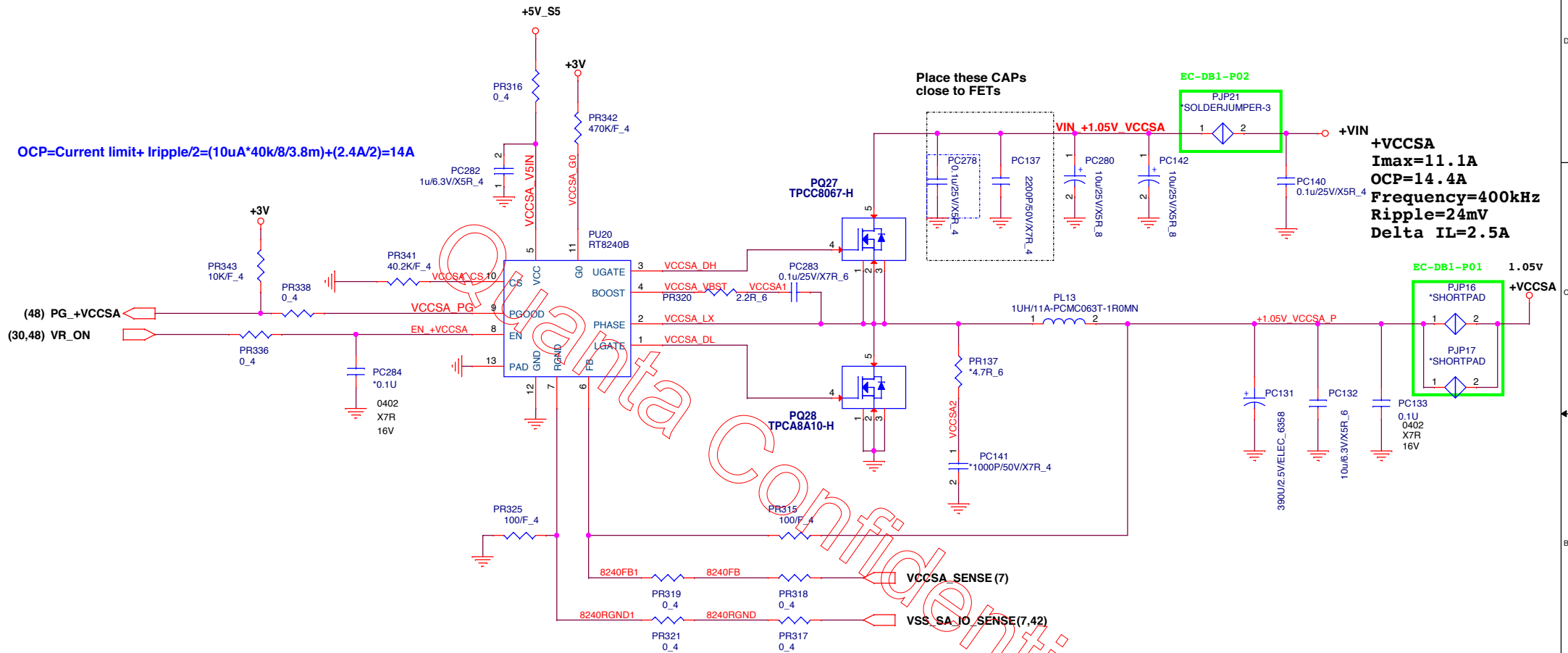
Title	+VCCIO(NB681)		
Size	Document Number	Rev	A
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Page Modified:	Thursday, December 17, 2015	Sheet 42 of 61	1



**Project: HP-SAIPAN**

Size	Document Number	Rev
	11	A

Page Modified: Thursday, December 17, 2015 Sheet 43 of 61

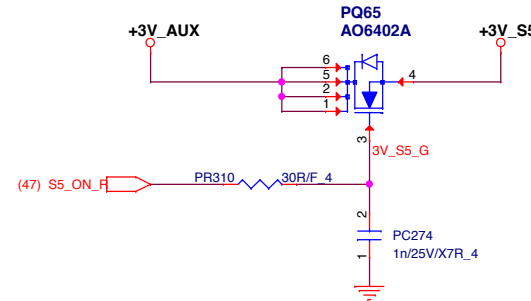




## S5 ON Load SW

AO6402A  
Rdson=24m@10V Vgs  
Imax=5.5A  
Pd: 0.726W

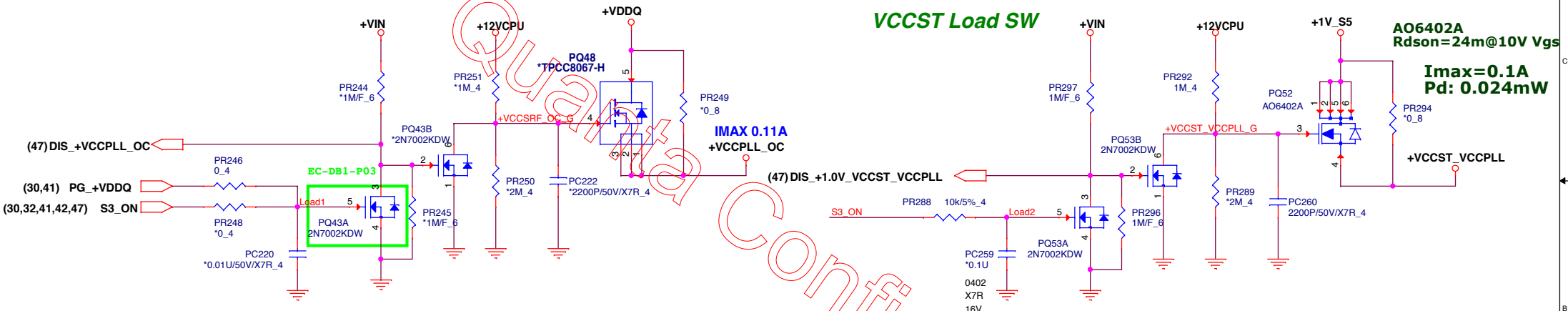
46



## VCCST Load SW

## VCCST Load SW

AO6402A  
Rdson=24m@10V Vgs  
Imax=0.1A  
Pd: 0.024mW



## MAIN ON\_1 Load SW

AO6402A  
Rdson=24m@10V Vgs

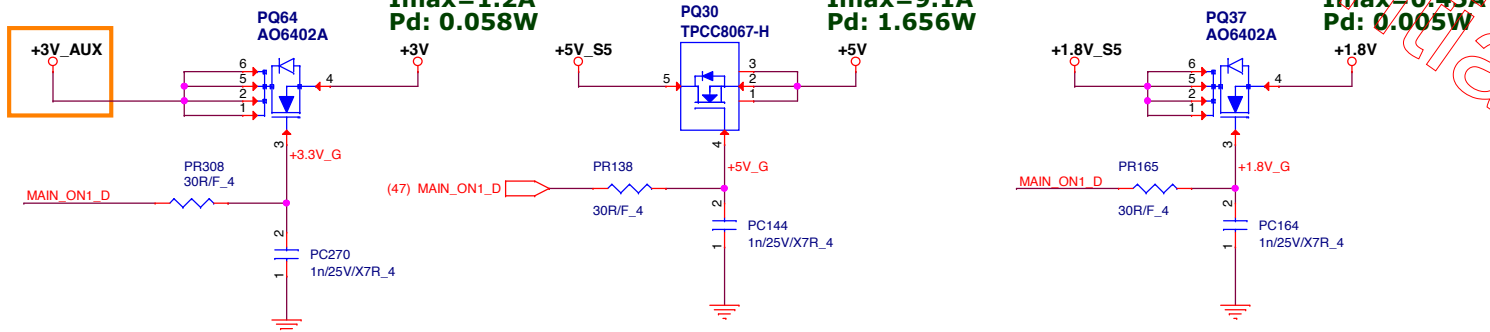
TPCC8067-H  
Rdson=20m@10V Vgs

AO6402A  
Rdson=24m@10V Vgs

Imax=1.2A  
Pd: 0.058W

Imax=9.1A  
Pd: 1.656W

Imax=0.45A  
Pd: 0.005W



## Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
ME3424D-G	TSOP-6	5.0A/6.7A	42m	+/- 20V
TPCC8067-H	3x3	9A	26m	+/- 20V
TPCA8064-H	SO-8	20A	7.9m	+/- 20V

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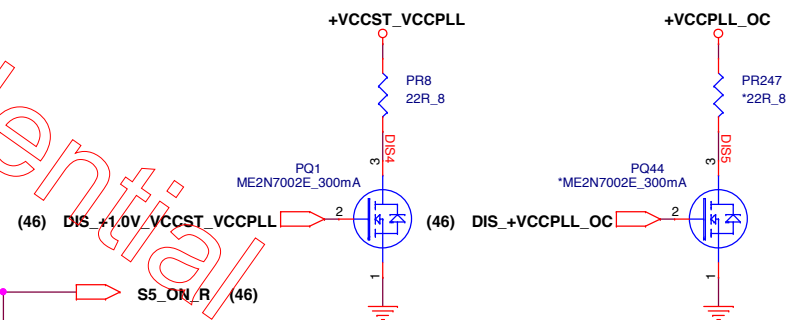
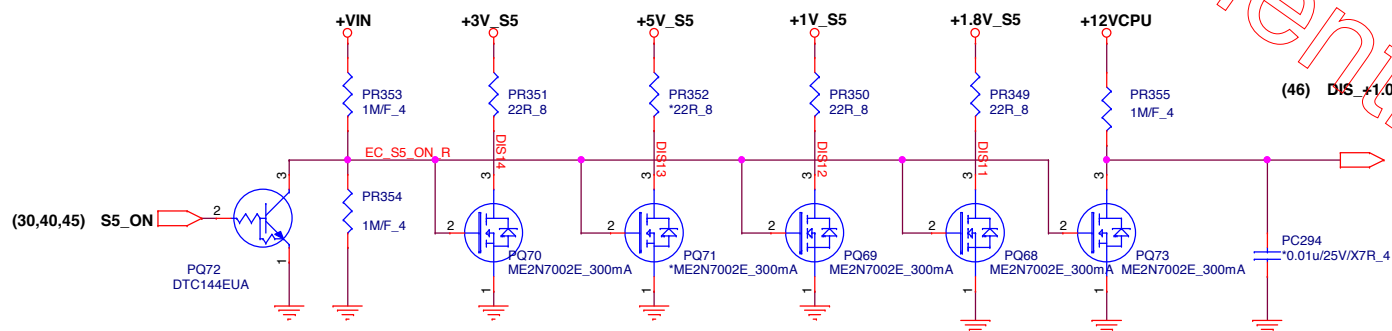
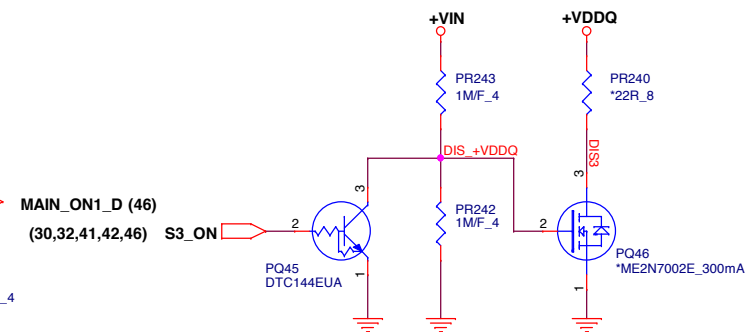
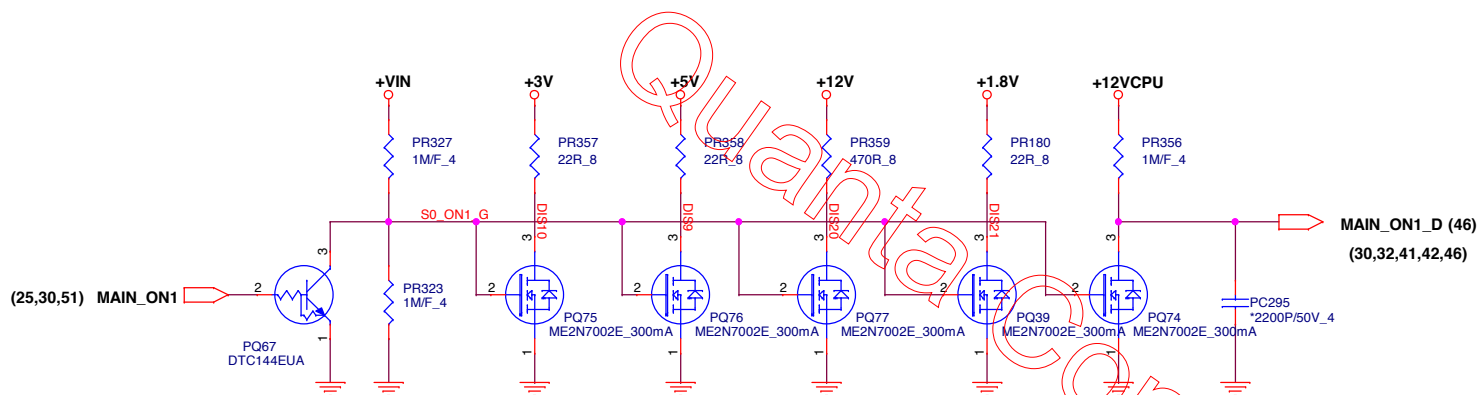
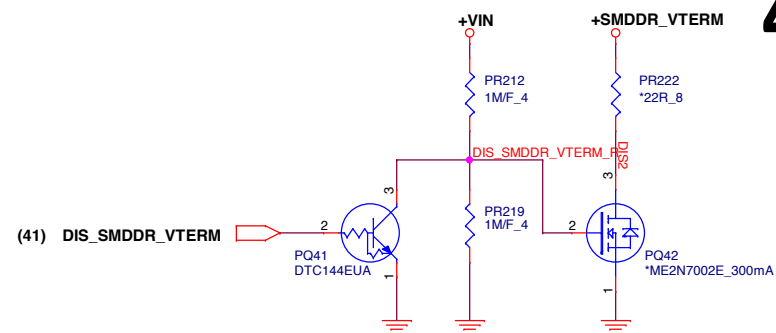
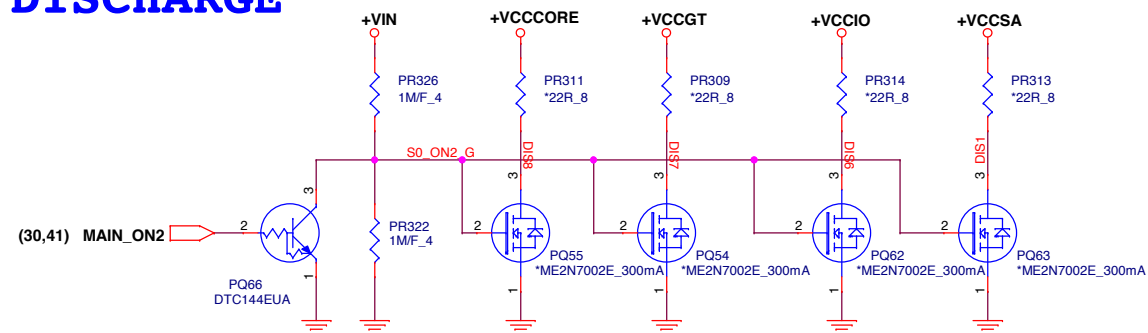
Project: HP-SAIPAN

Title	Load Switch		
Size	Document Number	Rev	
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Page Modified: Thursday, December 17, 2015 Sheet 46 of 61

# DISCHARGE

47



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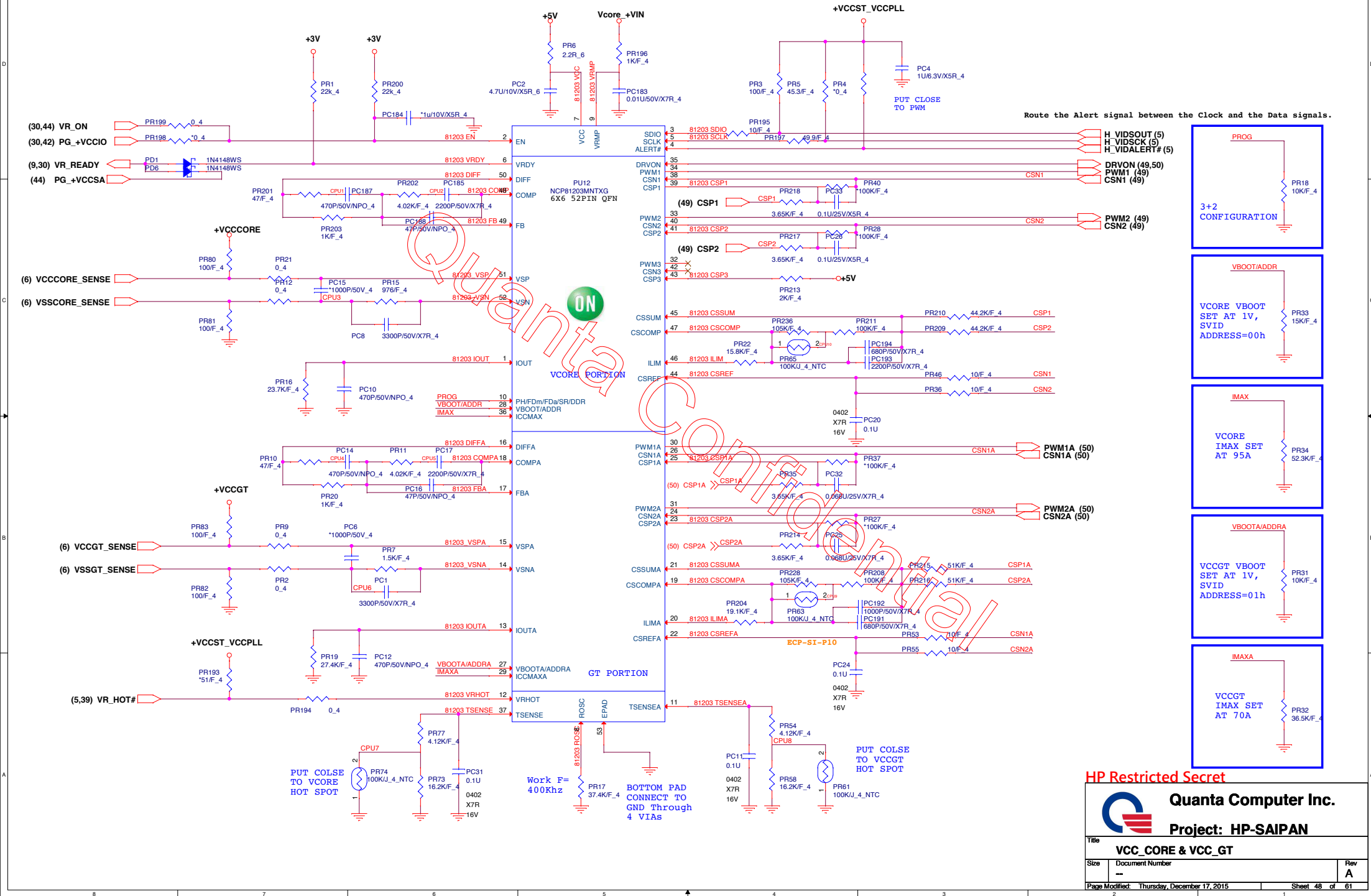
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Project: HP-SAIPAN

Title	Discharge		
Size	Document Number	Rev	A
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Page Modified: Thursday, December 17, 2015		Sheet 47 of 61	



## 48



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**Project: HP-SAIPAN**

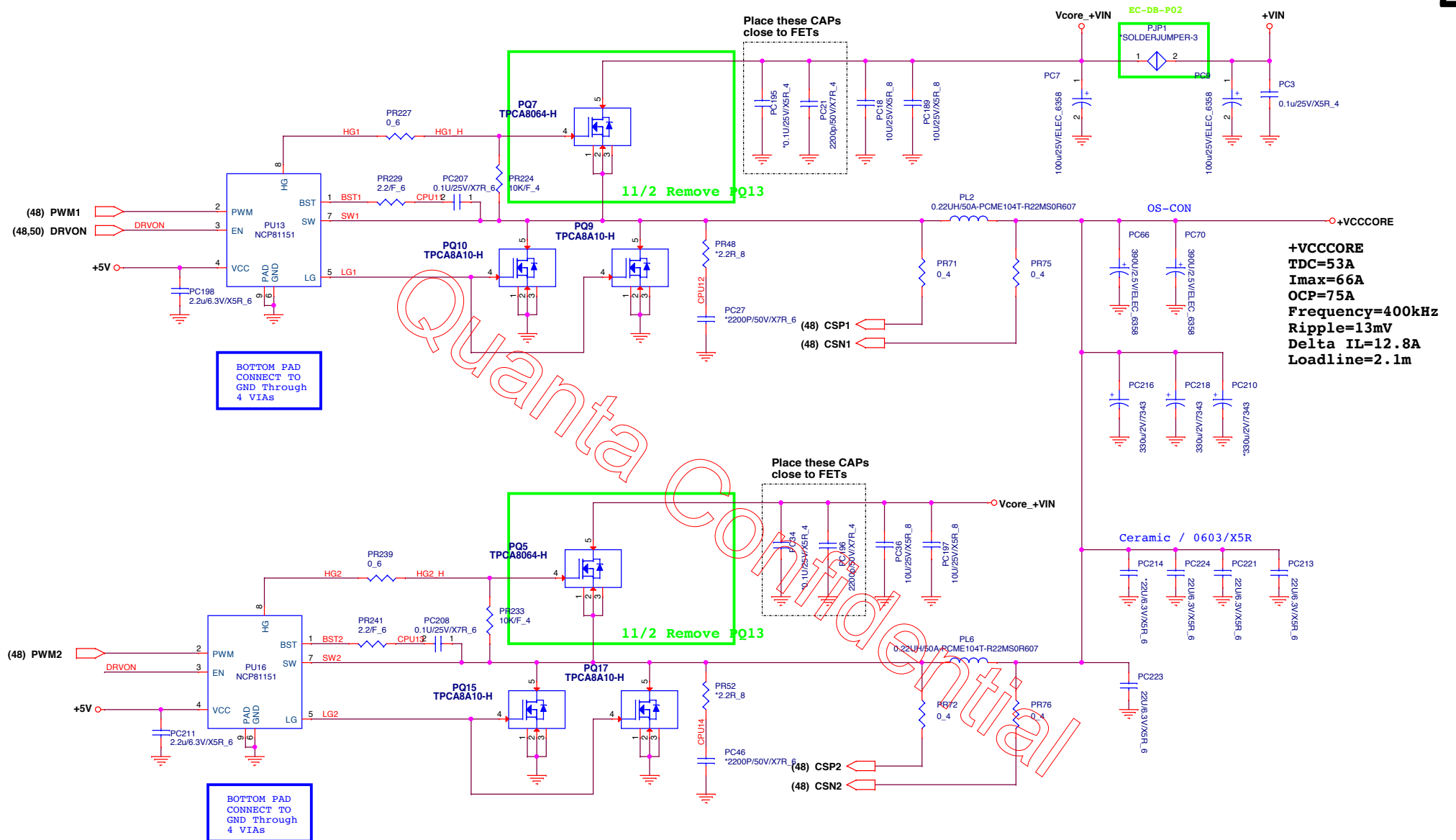
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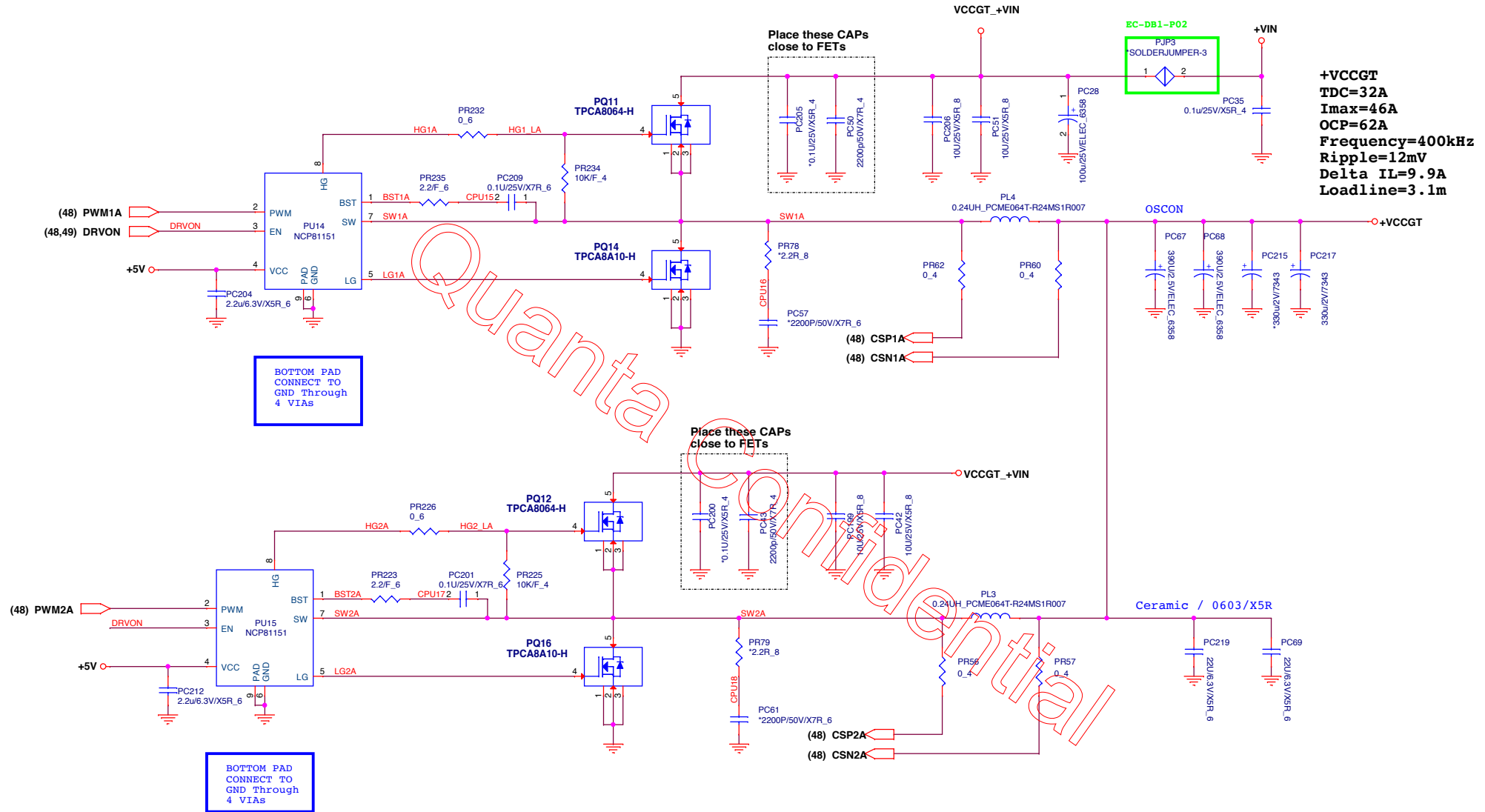
Size	Document Number
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Rev  
A

Page Modified: Thursday, December 17, 2015

Sheet 49 of 61





HP Restricted Secret

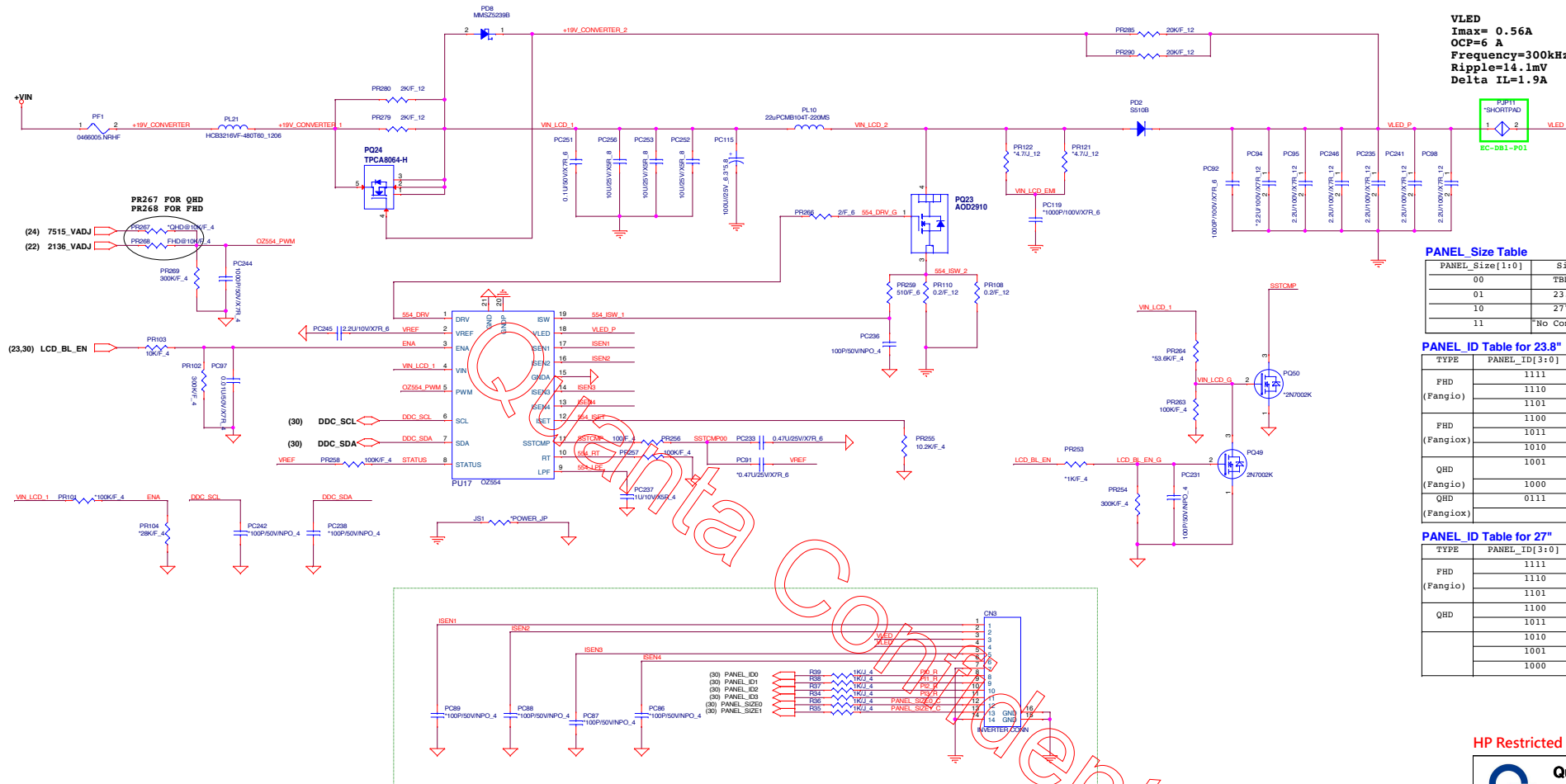


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Project: HP-Saipan

Title <b>VCCGT OUTPUT STAGE</b>		
Size	Document Number	Rev A
Page Modified: Thursday, December 17, 2015		
Sheet 50 of 61		



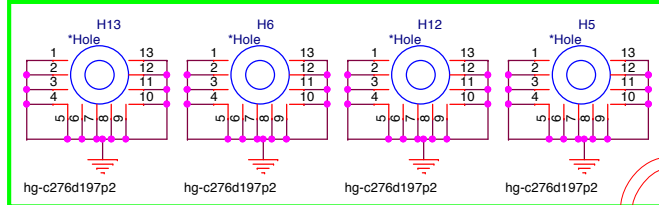
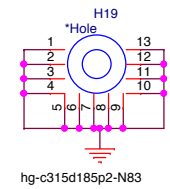
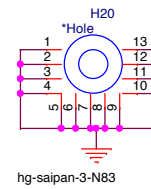
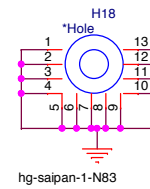
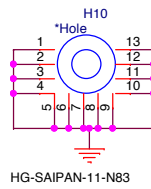
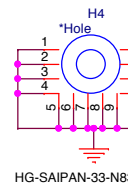
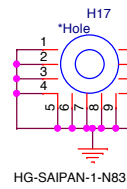
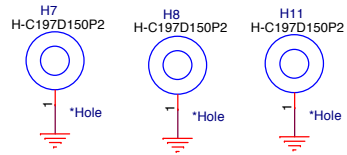






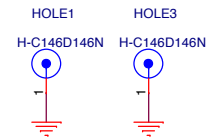


## CPU HOLE

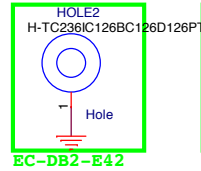


EC-DB2-E41

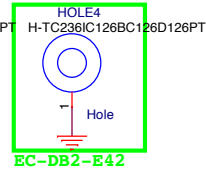
## VGA HOLE



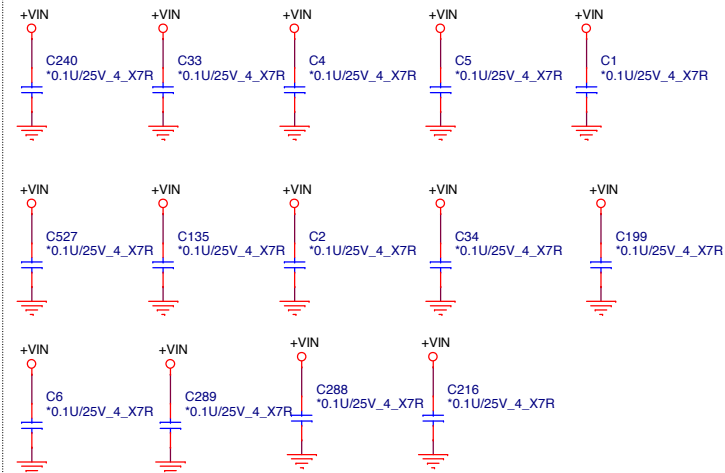
## WLAN HOLE



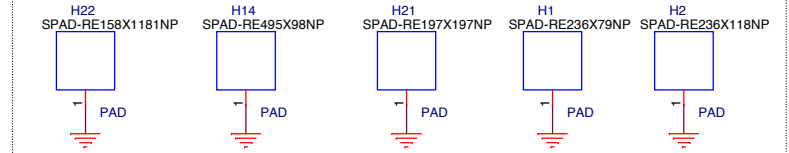
## SSD HOLE



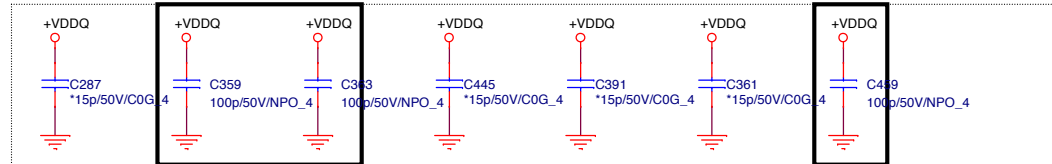
## Place around +VIN trace



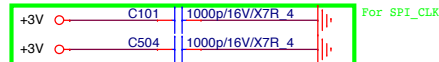
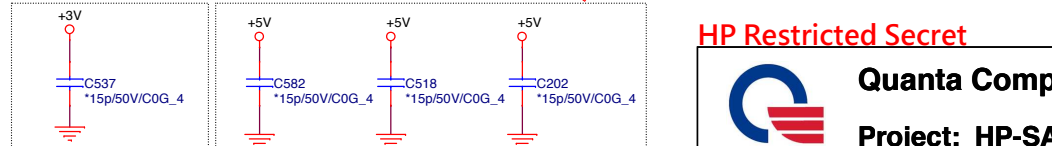
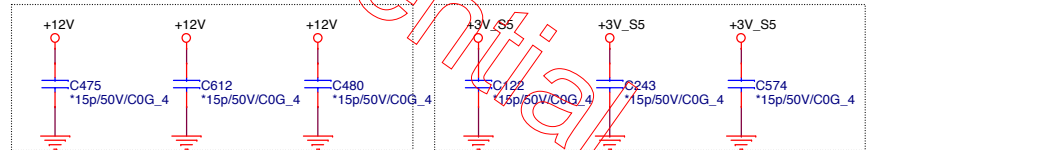
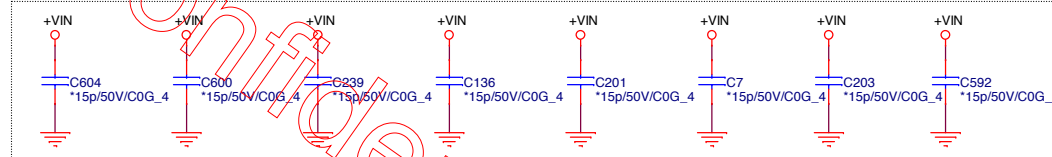
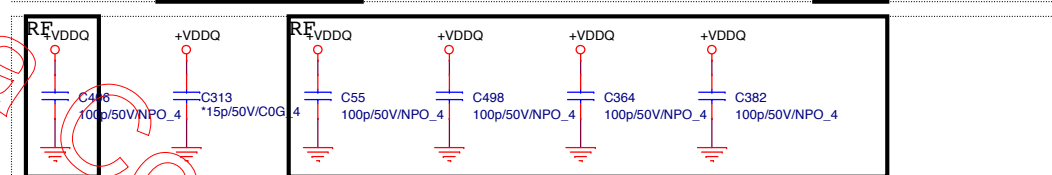
## EMI PAD



## RF



## RF



For SPI\_CLK

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Title  
HOLE/VIN CAP/RF CAP

Size Document Number

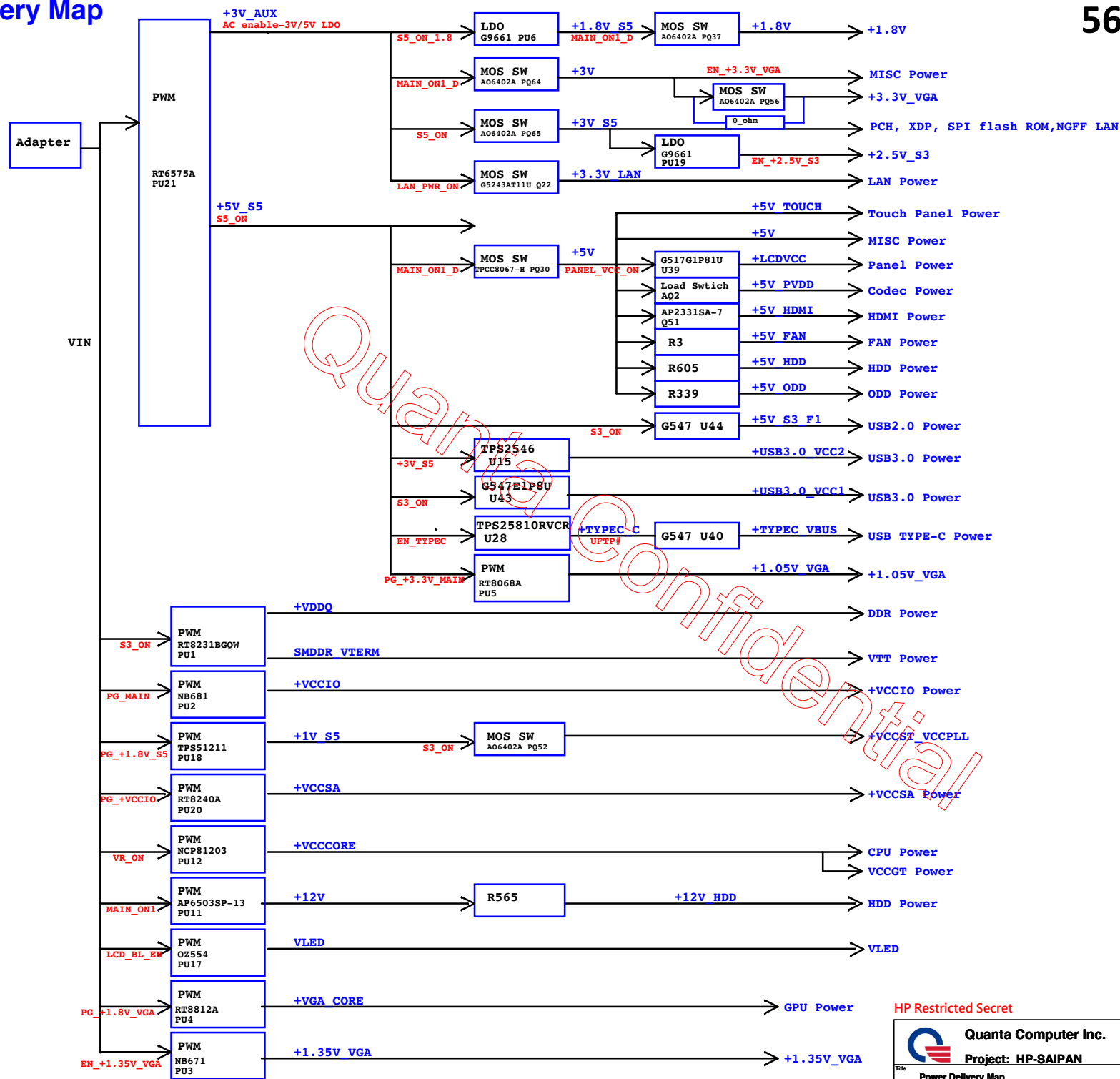
Rev  
B

Page Modified: Thursday, December 17, 2015

Sheet 55 of 61

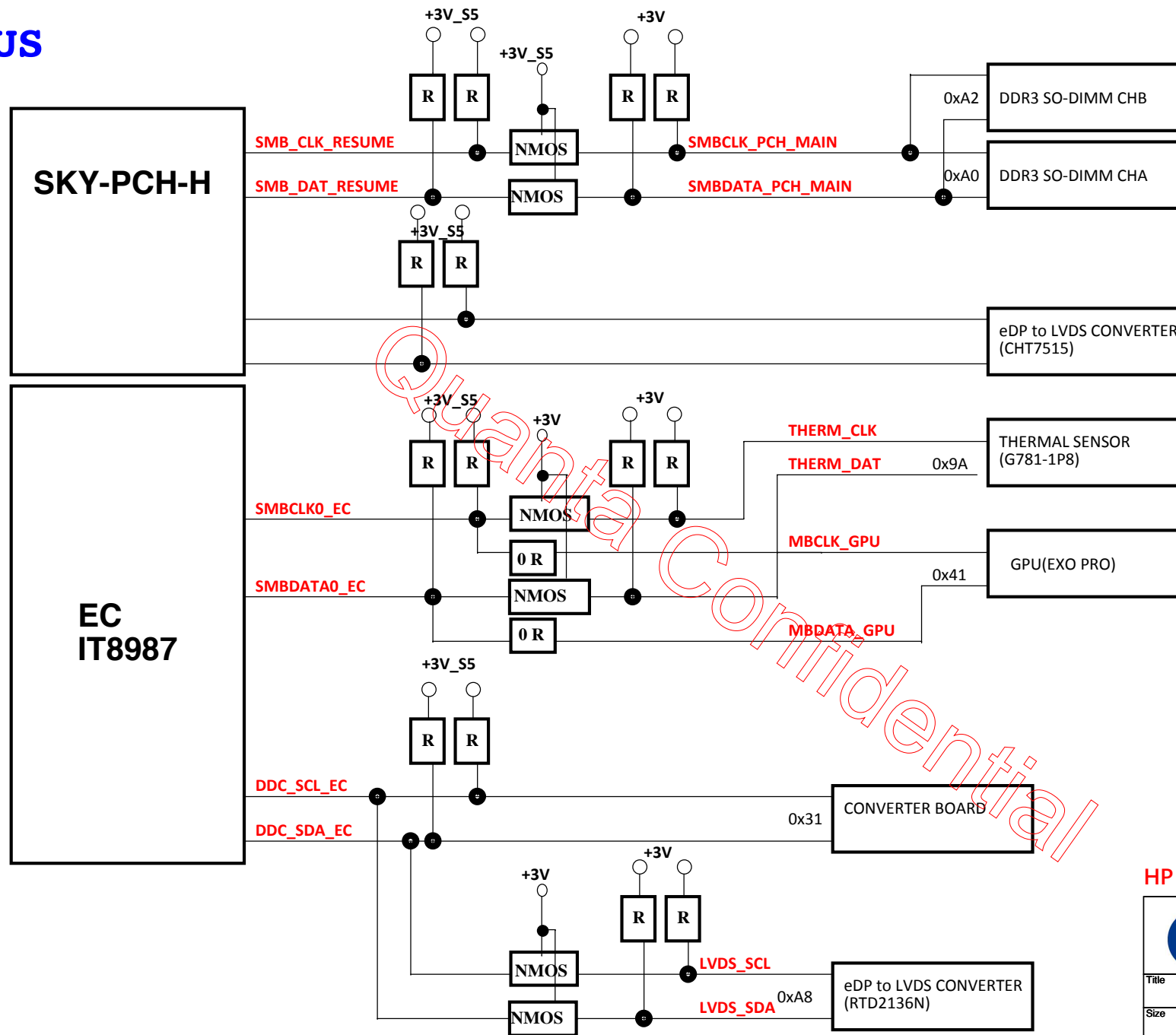
# Power Delivery Map

56



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Project: HP-Saipan	
Title	Power Delivery Map
Size	Document Number
Rev	A
Page Modified: Thursday, December 17, 2015	
Sheet 56 of 61	



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Title

SMBus

Size

Document Number

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Rev

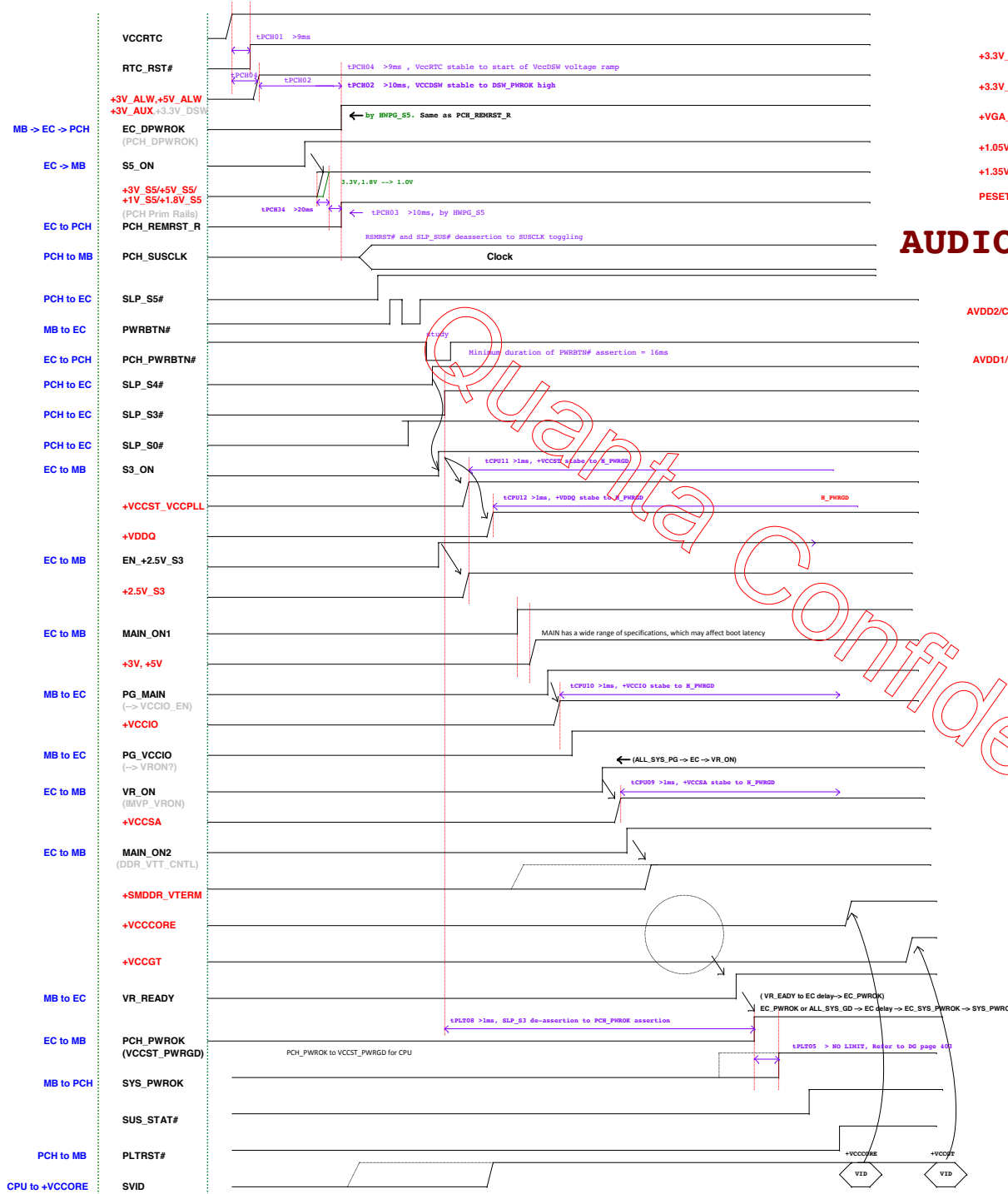
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Page Modified: Thursday, December 17, 2015

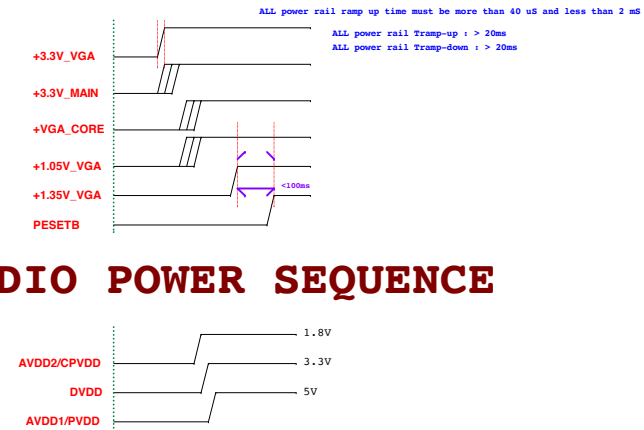
Sheet 57 of 61

# SKY- POWER SEQUENCE

# Nvidia dGPU POWER SEQUENCE 58

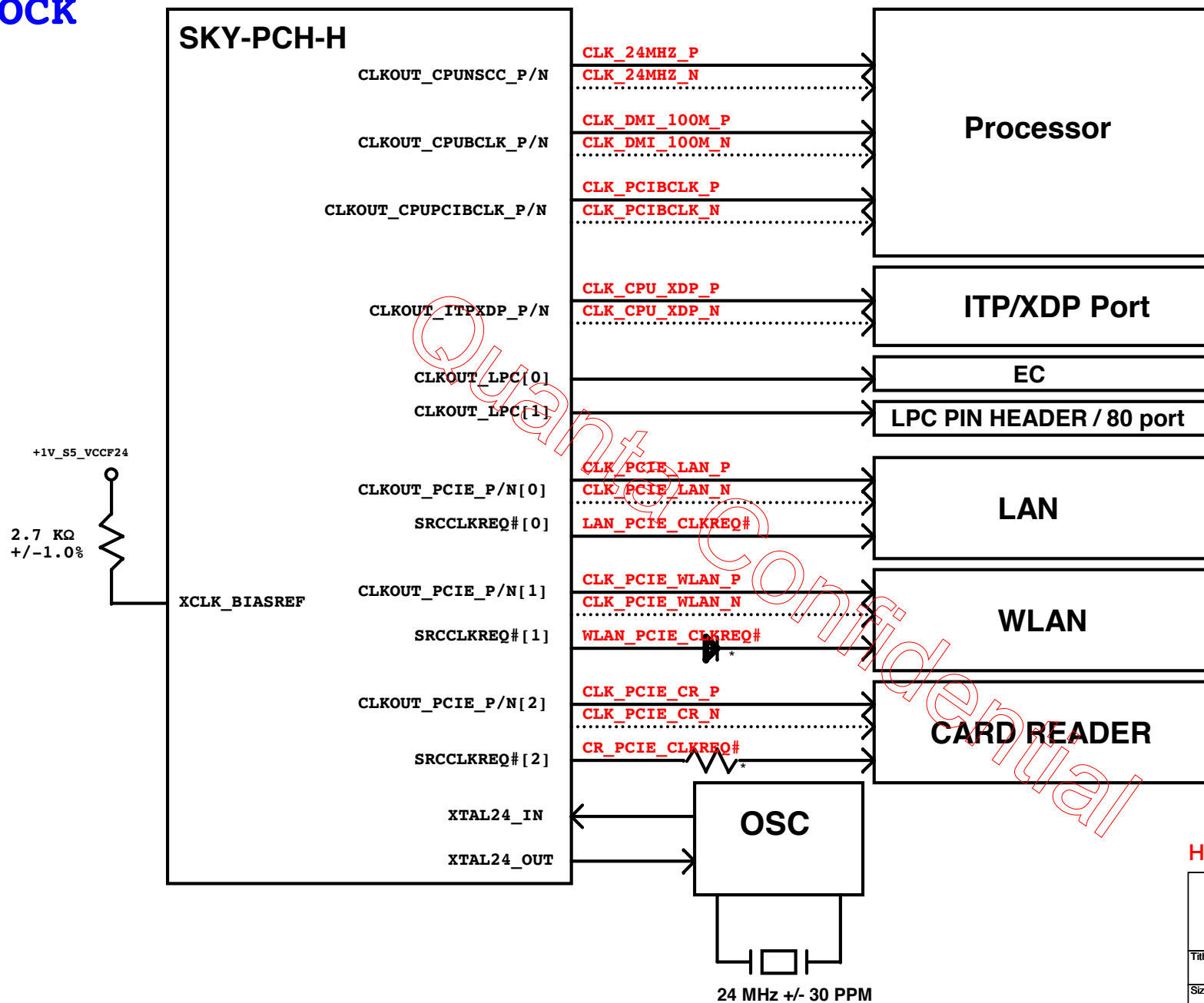


## AUDIO POWER SEQUENCE



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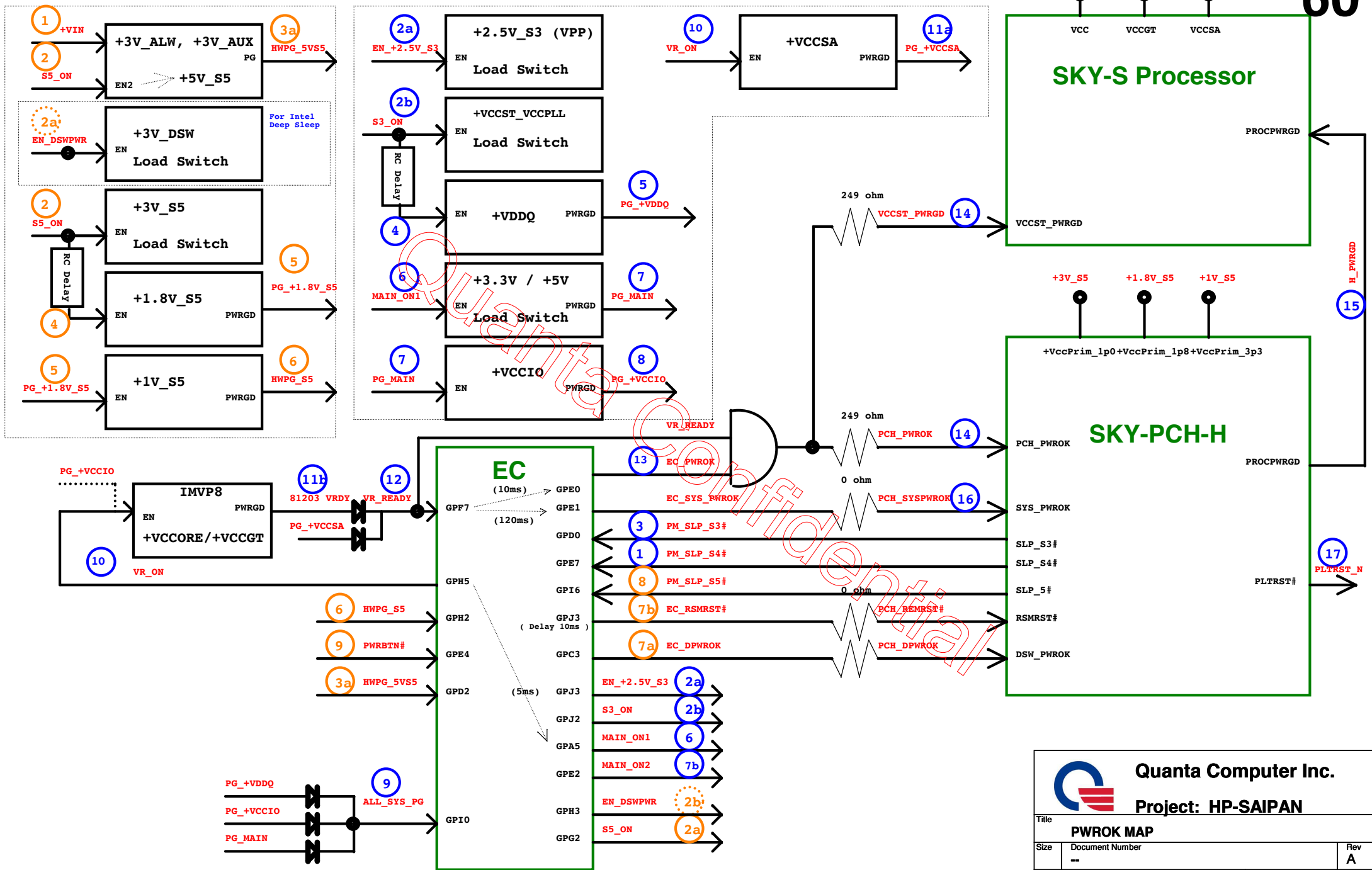


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Project: HP-SAIPAN

Title <b>CLOCK MAP</b>		
Size	Document Number	Rev
---	---	A
Page Modified: Thursday, December 17, 2015		
Sheet 59 of 61		

# PWROK MAP / RSMRST\_PWRGD#



## DB1 Change List

61

No.	Change details	Location/Description	Page	Change Reason
EC-DB1-E01	Change 0 ohm to shortpad	R76,R328,R329,R785,R166,R158,R732,R618,R351,R352,R358	5,9,10,12,16,26,34	Reduce 0 ohm usage for SMT.
EC-DB1-E02	Modify PEG HW straps	R489,R5106,R514	5	For PEG PCIe x4 Gen3 setting.
EC-DB1-E03	Remove AC caps on PEG [4:7] for N16S	C74,C73,C483,C479,C75,C76,C488,C497,C77,C78,C500	16	N16S-GMR support PEG x3 only.
EC-DB1-E04	Add dual mosfet on SMBI_CLK/DAT	C56,C73,C80,C567,C515	9	I2C power domain.
EC-DB1-E05	Remove C328	C328,C330	14,15	for DDR4 reset timing
EC-DB1-E06	Remove R612	R612	16	Don't support GC6.0
EC-DB1-E07	Remove R126,R118,R109	R126,R118,109	16,19	unnecessary
EC-DB1-E08	stuff R96	R96	9	NV suggest
EC-DB1-E09	De-populate SPI ROM	R64,R72,R129,U9,R124C102	19	De-populate SPI ROM
EC-DB1-E10	Change QHD panel circuit	all page	25	Chage QHD VCC control circuit
EC-DB1-E11	Chage R711 to 470 ohm	R711	25	QHD VCC discharge resistor
EC-DB1-E12	Change part	F9	26	common part
EC-DB1-E13	DMIC I2C circuit wrong	AR5/AR17/AR6/AR13	27	DMIC I2C circuit wrong
EC-DB1-E14	Change EC HW straps power domain to +3V_ALW	'--	30	timing issue
EC-DB1-E15	Stuff R571/R572	R571/R572	30	I2C power domain.
EC-DB1-E16	Remove R70	R70	30	Reduce 0 ohm usage for SMT.
EC-DB1-E17	Change +3.3V to +3.3V_CCD on CN4.1 & U3.5	CN4.1 & U3.5	31	To disable DMIC device in Fangio-x
EC-DB1-E18	Stuff U5,U4	U5,U4	31	ESD
EC-DB1-E19	Remove R3	R3	30	unnecessary


EC-DB-P01	change footprint to short pad.	PJP2,4-9,11-20,22-31	50-54	change footprint to short pad.
EC-DB-P02	change footprint to short pad.	PJP1,3,10,21	50-54	change footprint to short pad.
EC-DB-P03	change part reference for schematic error	PQ43A,PQ78A,PQ78B,PQ79A,PQ79B	50-55	change part reference for schematic error
EC-DB-P04	For Common parts	PQ29A,PQ29B		For Common parts

## DB2 Change List

No.	Change details	Location/Description	Page	Change Reason
EC-DB2-E01	Change 0 ohm to shortpad	R552,R761,R735,R316,R307,R706,R164,R336	5,9,10,11,22,34	Reduce 0 ohm usage for SMT.
EC-DB2-E02	Adding TVS DIODE	R666,R306,R278,R324,136,R781,R667,R231,R703,R372	5,14,34	ESD request
EC-DB2-E03	Change location C378/C379 to PC329/PC330	D6,D7	6	power parts.
EC-DB2-E04	Remove R673	R673	11	simple circuit
EC-DB2-E05	Stuff C594 10pf	C594	11	for CK 24M-EC timing
EC-DB2-E06	Change Board ID to SI ( STUFF R702)	R702	12	BOARD ID
EC-DB2-E07	ADD TVS on WLAN_PCIE_CLKREQ#	D46	12	ESD request
EC-DB2-E08	Change part	L58	18	For common part
EC-DB2-E09	Chage C71 to 10pf and C72 to 12pf	C71,C72	18	Xtal accuracy
EC-DB2-E10	Don't stuff R18/R20	R18,R20	21	unnecessary
EC-DB2-E11	Don't stuff C116	C116	22	unnecessary
EC-DB2-E12	Don't stuff R181 and add R822 pull down	R181,R822	22	Reatek recommend
EC-DB2-E13	Chage caps power rating from 16v to 10v	C108,AC9	22	Chage caps power rating
EC-DB2-E14	Chage C232 to and C228 to 8.2pf	C232/C228	24	Xtal accuracy
EC-DB2-E15	Change part	F9	26	For common part
EC-DB2-E16	Change Q10 to dual MOSFET. Q32/33 to Q57	Q10/Q11/Q10, Q32/Q33/Q57	26,34	Simple layout
EC-DB2-E17	Change part	AL9,AL10,AL11,AL13	27	For common part
EC-DB2-E18	adding disable DMIC icon	Aul.48	28	HP request
EC-DB2-E19	Stuff R803/R792/D33, don't stuff R802	R803,R802,R792,D33	12,28,29,34	enable PCIe clock request function
EC-DB2-E20	Adding M.2 SSD function	All page	35	HP request
EC-DB2-E21	Change RJ45 part	CN24	28	SMT request
EC-DB2-E22	Chage caps power rating from 10v to 6.3v	C230,C482,C495	29,34	Chage caps power rating
EC-DB2-E23	Stuff C666	C666	29	EMI request
EC-DB2-E24	Change GPIO table in EC	EN_TYPERC,CLR_CMOS,EN_AUDIO_PWD,BOX_BUTTON	30	common design
EC-DB2-E25	Change diode to 0 ohm	# R8377,EC_HVPS4,HWPS_5VPS	30	common design
EC-DB2-E26	Change SMI circuit	R837,R838,R839	30	unnecessary
EC-DB2-E27	Adding IRMT control pin	R517	30	IRMT
EC-DB2-E27	Adding IRMT control pin	R843	30	IRMT
EC-DB2-E28	Change QHD I2C control circuit	R627/R633	30	Leakage.
EC-DB2-E29	Remove D17/D19	D17/D19	30	unnecessary
EC-DB2-E30	Change L5 to 4.7ohm. Adding C674	L58,C674	31	DMIC EA timing
EC-DB2-E31	Stuff U5,U4	U5,U4	31	ESD
EC-DB2-E32	Add IRMT control circuit	R842,Q58,R840	31	IRMT
EC-DB2-E33	Reserve D45	D45	31	ESD
EC-DB2-E34	Change USB power switch	U43,U44,U33,U32,C342,C372	31,32	For common part
EC-DB2-E35	Change C235/C236 from 150uf to one 390uf (C236)	C235,C236	32	simple layout
EC-DB2-E36	Add M.2 SSD function	'--	35	HP request
EC-DB2-E37	Change Part	CN8	36	common design
EC-DB2-E38	Reserve C205	C205	36	Reserve only
EC-DB2-E39	Don't populate R384	R384	36	Leakage.
EC-DB2-E40	Remove LFC pin header	CN10	37	no enough layout space.

EC-DB-P01	change footprint to short pad.	PJP2,4-9,11-20,22-31	50-54	change footprint to short pad.
EC-DB-P02	change footprint to short pad.	PJP1,3,10,21	50-54	change footprint to short pad.
EC-DB-P03	change part reference for schematic error	PQ43A,PQ78A,PQ78B,PQ79A,PQ79B	50-55	change part reference for schematic error
EC-DB-P04	For Common parts	PQ29A,PQ29B		For Common parts

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		<b>Project: HP-SAIPAN</b>	
Title: <b>Change List</b>			
Size	Document Number	Rev	
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Page Modified: Thursday, December 17, 2015		Sheet: 61 of 61	